Design of cascaded all pass network with monotonous group delay response for broadband radio frequency applications

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Abstract: In this study, an iterative procedure is developed for designing radio frequency circuits with a specified group delay dispersion (GDD) characteristics over a broad bandwidth. Second order all pass networks (APNs) are cascaded systematically over multiple stages to achieve the same. The approach is flexible enough to design circuits for various group delay responses. This is demonstrated using two-stage APN with both positive and negative slopes of linear and non-linear group delay responses for a frequency band of 500 MHz–1 GHz. The proposed multi-stage design procedure is shown to help extend the bandwidth over which a uniform resolution of frequency discrimination is possible. Practical limitations in implementing this circuit are addressed while developing the prototype. The circuit is realised as a surface mount device-based implementation of modified two-stage APN. The realised circuit has a GDD of −6 ns/GHz and an insertion loss of 1.2 dB for 500 MHz–1 GHz band. The performance parameters such as GDD, insertion loss and device footprint of the proposed approach are significantly better than previously reported.

1 Introduction

Circuits and components that control group delay dispersion (GDD) have been used at audio to optical frequencies for wide range of applications including delay equalisation [1], chirp waveform generation [2, 3], signal analysis such as spectrum sniffing [4], chipless radio-frequency identification [5], compressive receivers [6] and pulse compression [7]. On passing through a GDD system, the signal experiences expansion of the pulse width, reduction of its peak amplitude and a temporal displacement of the spectral components [8, 9]. In particular, frequency discrimination [10–12] and real-time spectrum analysis [13] require uniform displacement of the spectral components. This can be obtained by a linear group delay with GDD which offers uniform group delay variation over the entire operational frequency band.

GDD control at optical frequencies has been realised using fibre optic components and structures [14]. Linear chirped fibre Bragg gratings (LCFGs), which are designed by varying the periods of effective refractive index modulation, are employed as dispersive delay lines [15]. They also find applications at radio frequency (RF) where a high operational bandwidth is achieved at the cost of high conversion loss, size and limitations in integration [16]. Chirped electromagnetic band gap structures are developed as an RF counterpart of LCFG where GDD is varied by changing the strip width along the length to induce Bragg like local reflection [17]. The bandwidth and dispersion achieved are size dependant. The structure has high loss and requires a coupler for system integration [17].

Components demonstrating RF GDD using various technologies are compared for performance parameters in [6, 12]. An ideal design requires independent control over the magnitude of loss characteristics and dispersion in group delay response, which can be achieved by all pass networks (APNs). Hence, APNs are explored as one of the technologies aimed at broadband group delay engineering. The distributed APNs are implemented as cascaded commensurate and non-commensurate C-sections [12, 18]. Commensurate C-sections have been used extensively and a detailed synthesis procedure for three-stage implementation is presented in [18] for specific delay responses. In a recent work, multi-stage edge-coupled non-commensurate C-section has been realised [12] to obtain group delay response over wideband. As no generalised closed-form analytical procedure is available for the synthesis of cascaded C-sections with a required GDD, they are designed using

optimisation procedures [12]. An iterative design is also developed for the synthesis of quasi-arbitrary delay response in [19]. However, it is restricted to frequencies within octave bandwidth. The APN implemented using distributed components in [12, 19] can be used to obtain responses where group delay value increases with increasing frequency (positive slope in group delay response). It requires additional circuitry for slope inversion [12] for many practical applications [6, 12]. The design flexibility of C-sections is compromised by high device footprint, especially at sub-gigahertz frequencies. For edge coupled C-sections, the coupling factor is limited by the fabrication considerations as the minimum distance between the lines is restricted [12, 20]. Thus, in practical implementations, the coupling factor is limited to a low value, limiting the group delay slope over the bandwidth. To overcome this limitation, the C-sections have been broadside coupled [21]. However, the loss in transmission line would result in large attenuation.

At audio frequencies, APNs have been extensively used as group delay equalisers for high fidelity audio amplification. The synthesis procedure for the lumped element APNs is well known at audio frequencies [1, 22–24] using various approximation methods. They are employed to design multi-stage APNs even for broadband responses. However, most of these use operational amplifier for compensating realistic component values and to achieve the required responses [1]. Group delay synthesis using lumped APN circuits have also been demonstrated in [25, 26] for negative group delay response using active circuit topologies. In contrast, the above applications [1–17] require RF circuits with specified GDD characteristics. Component losses cause the transfer function poles and zeros of the RF APNs to shift [27]. Thereby, the network no longer posses the all pass responses. Implementation of RF APNs using lumped components is limited by the Q factor, tolerance and component parasitic [3, 28, 29] and is rarely followed.

In this paper, an iterative procedure is proposed to design broadband circuits for monotonous group delay response at RF. Second-order APNs using lumped components are used as basic building blocks for ideal circuit design. They are systematically cascaded to achieve various candidate group delay responses with both positive and negative slopes. As a proof of concept, the design is implemented using commercial surface mount device (SMD) components considering the practical implementation challenges and limitations such as component availability, tolerance, finite Q factor

and mounting pads. SMD-based circuit implementations are common for RF applications up to about 5 GHz.

The paper is organised as follows. In Section 2, an iterative design procedure is developed for multi-stage APN design with desired overall response. The outcome of this iterative procedure is a circuit synthesis that has minimum deviation in the group delay response over a broad bandwidth. Examples of two-stage APN design are discussed to obtain different group delay responses for $f = 0.5$ to 1 GHz. Multi-stage design example is shown for a linear group delay response over an extended bandwidth. Linear group delay response with different GDDs is also shown using a two-stage APN design. In Section 3, design implementation using lumped SMD components is developed and effect of component Q factor on performance parameters is considered. GDD circuits in the above operational band assume significance in the context of software defined radios and cognitive radios [29]. In Section 4, hardware measurement results for two-stage APN circuit with negative slope linear group delay response are presented. They are further compared with distributed circuits for various performance parameters.

2 Design procedure

As discussed above, lumped component multi-stage APN has the potential to provide high GDD monotonous group delay response over a broad bandwidth at RF. In this section, we formulate the iterative procedure followed for designing these circuits.

2.1 Group delay of APN

Lumped element APN of any order can be realised by cascading the first- and second-order APNs [27, 30]. They can be cascaded without any interaction as their terminal impedances are characterised by the constant resistance property. The total delay of the cascaded APN will be the sum of individual stage delays at a frequency. The second-order APN is characterised by two design parameters – resonance frequency ω_r and coefficient k, which may take values in the range (0, 1) [27, 30]. The group delay response in terms of the design parameters is given by

$$\mathrm{GD}(\omega) = \frac{2k\omega_r(\omega_r^2 + \omega^2)}{(\omega_r^2 - \omega^2)^2 + k^2\omega^2\omega_r^2} \qquad (1)$$

The group delay is positive and often varies as a non-linear function of frequency and is symmetric with a peak at ω_r. The response is made broad or sharp by variation in k. The parametric variation of delay response with respect to ω_r and k is given in [27, 29, 30]. A constant group delay can be obtained over a wide frequency range at the trailing edges of the delay response but a non-constant linear group delay is obtained only as a linear approximation over a narrow band of frequencies. Monotonous Gaussian and quadratic group delay responses are a function of ω^2, yet a desired broadband frequency spread for these responses cannot be directly obtained from single-stage APN. Therefore, multiple stages have to be cascaded with appropriate choice of ω_r and k to obtain these delay responses over broad frequency range.

2.2 Design procedure for multi-stage APN

The specifications for the design are monotonous group delay response $\mathrm{GD}_{\mathrm{spec}}(\omega) > 0$ over the operational bandwidth $\omega = \{\omega_1, \omega_2\}$ and maximum error $\varepsilon_{\mathrm{spec}}$. The design parameters to be determined are the number of stages N, resonance frequencies $\{\omega_{r1}, \omega_{r2}, \ldots, \omega_{rN}\}$ and coefficients $\{k_1, k_2, \ldots, k_N\}$. Group delay responses of individual stages are $\{\mathrm{GD}_1(\omega), \mathrm{GD}_2(\omega), \ldots, \mathrm{GD}_N(\omega)\}$. For convenience, a factor X is defined for the N stages $\{X_1, X_2, \ldots, X_N\}$, where X_N determines the contribution of stage N to the peak value of the target group delay that has to be achieved by each stage. The start value of X_N is taken as 1.

The normalised error between the designed group delay $\mathrm{GD}_{\mathrm{design}}(\omega)$ and specified group delay $\mathrm{GD}_{\mathrm{spec}}(\omega)$ is given by

$$\varepsilon(\omega) = \left| \frac{\mathrm{GD}_{\mathrm{spec}}(\omega) - \mathrm{GD}_{\mathrm{design}}(\omega)}{\mathrm{GD}_{\mathrm{spec}}(\omega)} \right| \qquad (2)$$

The partial derivative of the difference $\varepsilon(\omega)$ with respect to design variables $\{\omega_{r1}, \omega_{r2}, \ldots, \omega_{rN}\}$ and $\{k_1, k_2, \ldots, k_N\}$ must be zero for optimum design. However, the non-linear relationship among the variables prevents the analytical solution of the system of equations [27]. Therefore, an iterative approach is used for multi-stage APN design and is shown in Fig. 1a. The approach is based on a single-stage perspective with addition of individual stages to obtain multi-stage APN with required group delay responses over broadband.

For the proposed applications in [1–17], circuits with GDD are required. GDD is the derivative of the group delay with respect to angular frequency and is characterised by the slope of the group delay response. The resonance frequency ω_{r1} is the end frequency of the operational band ω_2 or ω_1 for monotonous increasing/decreasing group delay response (positive/negative slope response)

$$\omega_{r1} = \begin{cases} \omega_1, & \text{negative slope } \mathrm{GD}_{\mathrm{spec}}(\omega) \\ \omega_2, & \text{positive slope } \mathrm{GD}_{\mathrm{spec}}(\omega) \end{cases} \qquad (3)$$

The factor X_1 is defined and chosen such that $0 < X_1 \leq 1$

$$X_1 = \frac{\mathrm{GD}_1(\omega)}{\mathrm{GD}_{\mathrm{spec}}(\omega)} \bigg|_{\omega = \omega_{r1}} \qquad (4)$$

The coefficient k_1 is obtained by

$$k_1 = \frac{4}{\omega_{r1} X_1 \mathrm{GD}_{\mathrm{spec}}(\omega) \big|_{\omega = \omega_{r1}}} \qquad (5)$$

The total group delay of the APN with N stages is given by

$$\mathrm{GD}_{\mathrm{design}}(\omega) = \sum_{m=1}^{N} \frac{2k_m\omega_{rm}(\omega^2 + \omega_{rm}^2)}{(\omega_{rm}^2 - \omega^2)^2 + k_m^2\omega^2\omega_{rm}^2} + \mathrm{GD}_0 \qquad (6)$$

where GD_0 is the constant group delay added to increase the group delay to the required peak value. A small frequency of $\Delta\omega_{rn}$ may be added to ω_{rn} at each stage to compensate for the shift in peak for high value of k_n [30].

The individual APN stages are added and X_n is varied in the range (0, 1). The iteration is carried out until the condition

$$\mathrm{Max}(\varepsilon(\omega)) \leq \varepsilon_{\mathrm{spec}} \qquad (7)$$

is reached. The parameters of the subsequent APN stages are obtained as follows:
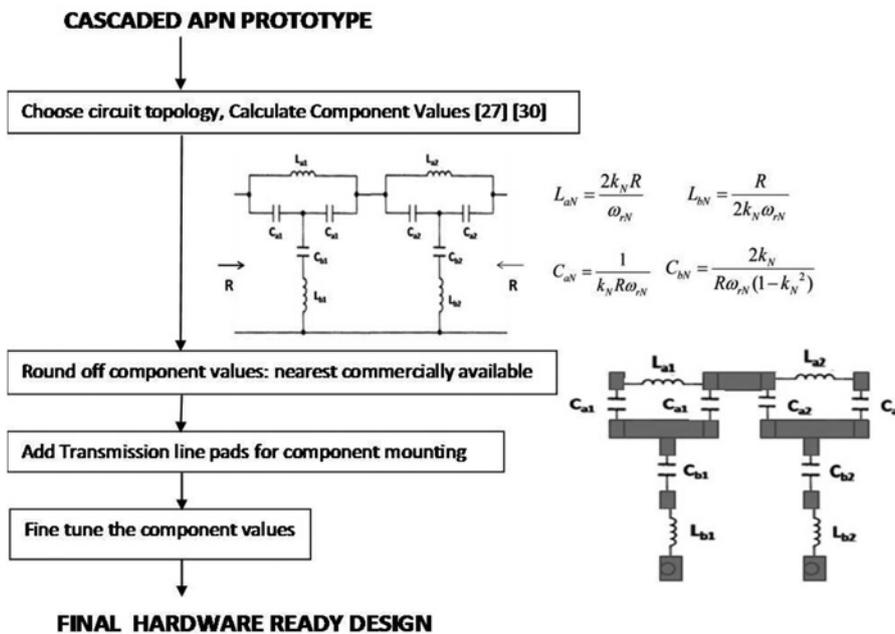
• The delay to be achieved by the nth stage $\mathrm{GD}_{n-1}^{\mathrm{sum}}(\omega)$ is the difference of specified group delay $\mathrm{GD}_{\mathrm{spec}}(\omega)$ and summation of group delays achieved by the previously designed $n-1$ stages and is given by

$$\mathrm{GD}_{n-1}^{\mathrm{sum}}(\omega) = \mathrm{GD}_{\mathrm{spec}}(\omega) - \sum_{m=1}^{n-1} \frac{2k_m\omega_{rm}(\omega_{rm}^2 + \omega^2)}{(\omega_{rm}^2 - \omega^2)^2 + k_m\omega_{rm}^2\omega^2} \qquad (8)$$

• The resonance frequency ω_{rn} is the frequency at which $\mathrm{GD}_{n-1}^{\mathrm{sum}}(\omega)$ has a peak value.
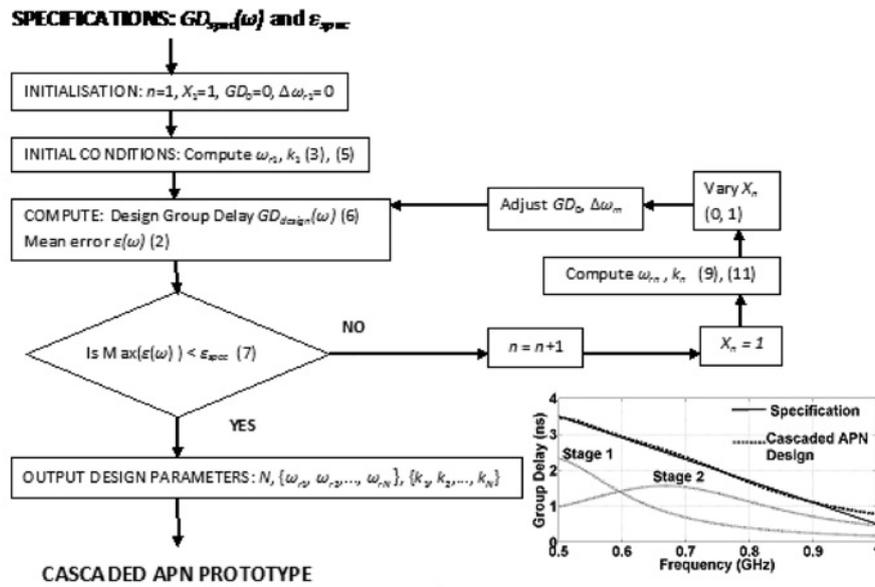
Fig. 1 *APN-based RF circuit design procedure for specified group delay response over broadband*
a Ideal component design of multi-stage APN using MATLAB (Section 2)
b SMD component design using ADS (Section 3)

- The appropriate choice of X_n is used to obtain k_n and is given by

$$X_n = \frac{\mathrm{GD}_n(\omega)}{\mathrm{GD}_{n-1}^{\mathrm{sum}}(\omega)}\bigg|_{\omega=\omega_{rn}} \tag{9}$$

- The parameter k_n is obtained by solving the quadratic equation

$$k_n^2 - k_n\left(\frac{2(\omega_{rn}^2 + \omega^2)}{X_n \omega_{rn}\omega^2 \mathrm{GD}_{n-1}^{\mathrm{sum}}(\omega)}\right) + \left(\frac{\omega_{rn}^2 - \omega^2}{\omega_{rn}\omega}\right)^2 = 0 \tag{10}$$

and choosing $k_n < 1$. The choice of $\{X_1, X_2, \ldots, X_N\}$ and GD_0 determine the error $\varepsilon(\omega)$. The designed and individual stage group delay responses to obtain a specified response for a two-stage design are shown graphically in Fig. 1a. The design parameters obtained by the above procedure are the number of stages N, the

resonance frequencies $\{\omega_{r1}, \omega_{r2}, \ldots, \omega_{rN}\}$ and coefficients $\{k_1, k_2, \ldots, k_N\}$. For circuit design, a bridged T topology is chosen for the individual APN stages based on the values of ω_r and k. The different network realisations of APN and the corresponding component design equations are given in [27, 30]. Components of the chosen network are ideal and can be implemented in any hardware technology. The co-simulation procedure for SMD implementation of the designed circuit is discussed in Section 3.

2.3 Design of two-stage APN for various candidate group delay responses

The design procedure in Section 2.2 has been implemented in MATLAB to achieve various group delay responses with both positive and negative slopes for a frequency band of $f = 0.5$ to 1 GHz. The mathematical functions [12] and design parameters

Table 1 Design parameters of two-stage APN for different group delay response, $\omega_0 = 2\pi$ Grad/s, $\Delta\omega = 0.4\pi$ Grad/s, $x = 1.5 \times 10^{-28}$, GD = 0.5 to 3.5 ns

Delay type		f_{r1}, GHz	k_1	f_{r2}, GHz	k_2
Gaussian GD(ω) = GD$_1$ + (GD$_2$ − GD$_1$)exp $^{-0.5(\omega-\omega_0/\Delta\omega)^2}$	positive slope	1.01	0.2555	0.86	0.4403
	negative slope	0.5	0.5305	0.69	0.4901
quadratic GD$(\omega) = \dfrac{\text{GD}_2 - \text{GD}_1}{\omega_2 - \omega_1}(\omega - \omega_1) + \text{GD}_1 + x(\omega - \omega_1)(\omega - \omega_2)$	positive slope	1.02	0.2392	0.87	0.5962
	negative slope	0.5	0.6110	0.63	0.7895
linear non-constant GD$(\omega) = \dfrac{\text{GD}_2 - \text{GD}_1}{\omega_2 - \omega_1}(\omega - \omega_1) + \text{GD}_1$	positive slope	1.02	0.2270	0.828	0.4362
	negative slope	0.5	0.5463	0.7	0.5955

obtained for two-stage APN for $\varepsilon_{\text{spec}} = 0.1$ are mentioned in Table 1. The designed group delay is compared with the candidate group delay responses in Fig. 2.

2.4 Design of two-stage APN for different GDD

The GDD of the circuit can be characterised by group delay slope (ns/GHz) [9, 11]. The two-stage design procedure can also be used to obtain linear group delay responses with different dispersion. The design parameters of the two-stage APN for $f = 0.5$ to 1 GHz and $\varepsilon_{\text{spec}} = 0.1$ are given in Table 2. The responses are shown in Fig. 3 along with the specified group delay responses.

2.5 Design of multi-stage APNs for extended bandwidth and GDD

The design procedure is used to obtain linear group delay between 0.5 and 3 ns over a frequency band $f = 0.5$ to 1.5 GHz. The design parameters are tabulated in Table 3 and group delay response is shown in Fig. 4. Hence, the procedure is validated to be designed over multiple stages to increase the absolute bandwidth.

The design can be further extended by cascading the above designed three stages to increase the GDD. The group delay responses of six-stage and nine-stage designs are also shown in Fig. 4.

2.6 Design of multi-stage APNs for extended bandwidth and error

The above design procedure can be readily extended for multiple stages to obtain a larger bandwidth $f = 1$ to 5 GHz [12]. Number of stages N to be cascaded to obtain a specified group delay response depends on the maximum error $\varepsilon_{\text{spec}}$ specified for the application. The simulation is carried out for $\varepsilon_{\text{spec}} = 0.01$ and 0.06. The design parameters are tabulated in Table 4. A reasonable response is obtained with a five-stage APN. It may also be observed from Fig. 5 that low $\varepsilon_{\text{spec}}$ increases the number of stages.

3 Implementation by co-simulation

In this section, a co-simulation-based procedure is employed to implement the multi-stage APN design to overcome limitations such as tolerance in the value of components and Q factor (losses)
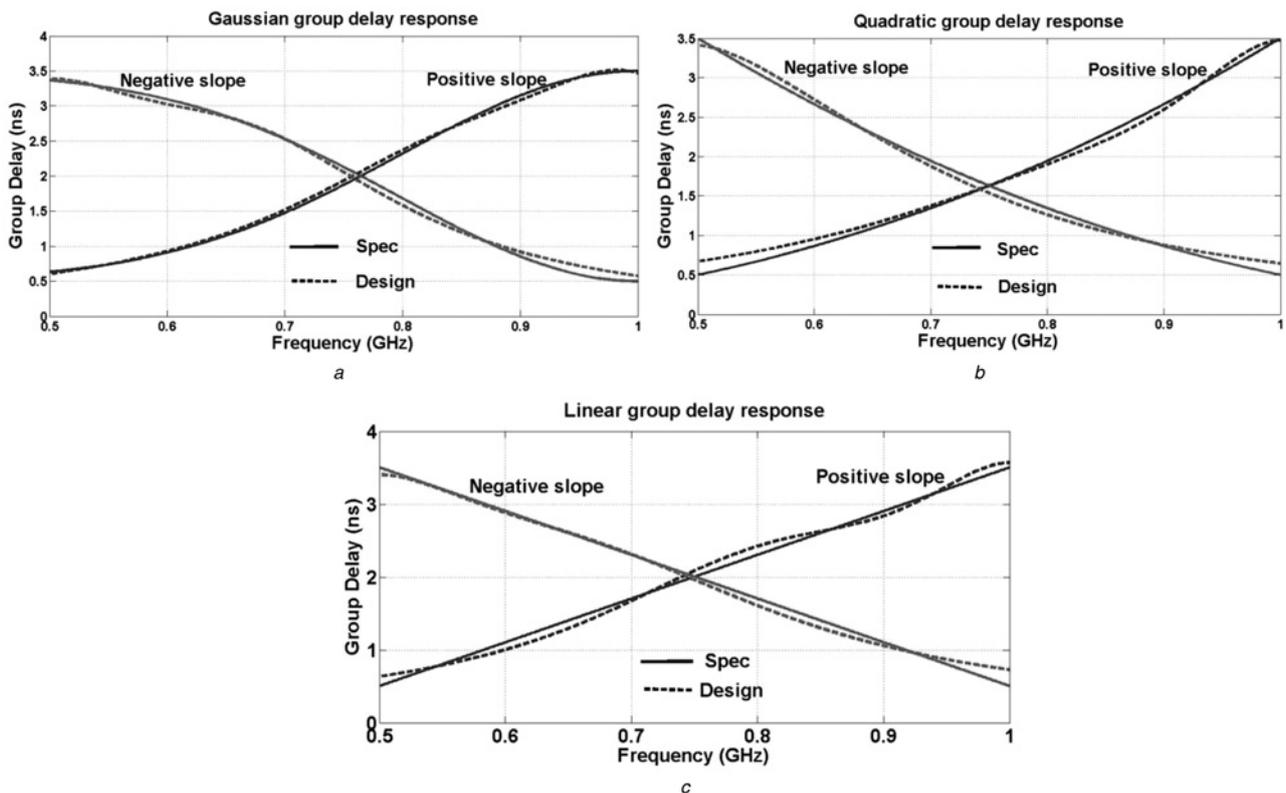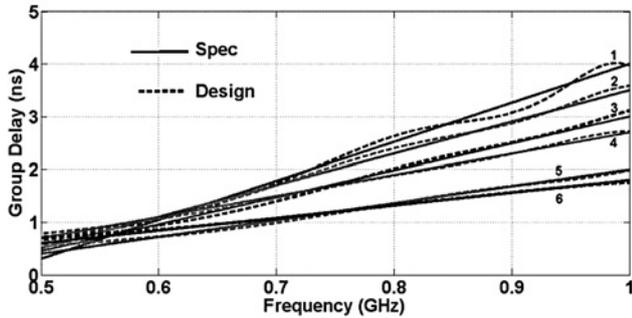

Fig. 2 Monotonous group delay responses of two-stage APN, specified and designed: positive and negative slopes
a Gaussian
b Quadratic
c Linear non-constant

Table 2 Design parameters of two-stage APN for different dispersion

Design no.	f_{r1}, GHz	k_1	f_{r2}, GHz	k_2	Group delay, ns	Slope, ns/GHz
1	1.01	0.2022	0.826	0.3864	[4–0.3]	7.4
2	1.02	0.2270	0.828	0.4362	[3.5–0.5]	6
3	1.05	0.2826	0.878	0.5139	[3–0.45]	5.1
4	1.03	0.35	0.860	0.6	[2.7–0.7]	4
5	1.15	0.2260	0.944	0.6004	[2–0.4]	3.2
6	1.2	0.6	1	0.68	[1.8–0.6]	2.4

Fig. 3 *Specified and designed linear group delay responses of two-stage APN with different GDD; design parameters in Table 2*

Table 3 Design parameters of three-stage APN for linear group delay response, $f = 0.5$ to 1.5 GHz

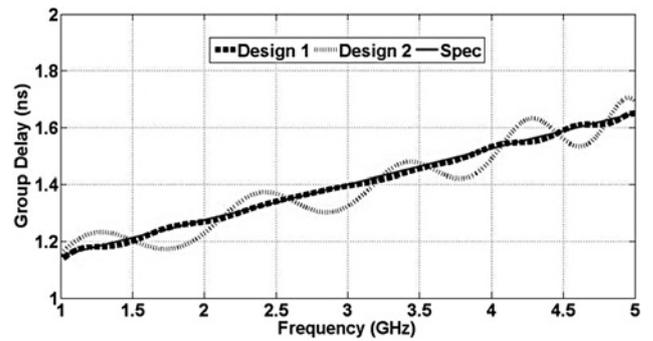| Stage	1	2	3
f_r, GHz	1.53	1.3	0.99
k	0.205	0.35	0.655
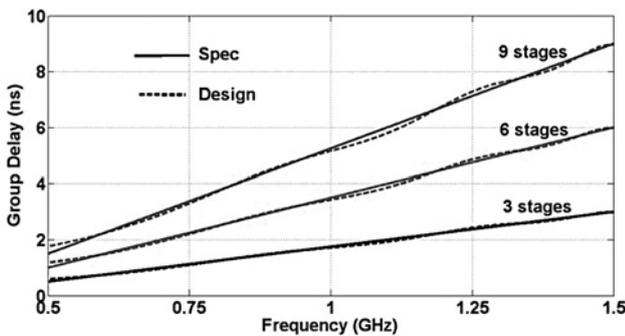
Fig. 4 *Linear group delay response of cascaded multi-stage APN*

due to technological limitations at RF. Component losses may cause the transfer function poles and zeros to shift to the left, causing the design in Section 2.2 to deviate from the all pass response. APNs with a small k are more sensitive as the transfer function zeros are closer to $j\omega$ axis [27].

The design and analysis is carried out in Agilent Advanced Design System (ADS2009) using momentum co-simulation. As an example,

Fig. 5 *Specified and designed linear group delay responses of multi-stage APN with different ε_{spec}*

Table 5 Ideal design and final component values of two stage design for linear negative slope group delay response

		L_a, nH	C_a, pF	L_b, nH	C_b, pF
ideal values: design Section 2	stage 1	17.389	11.653	14.567	9.9147
	stage 2	13.540	7.6361	9.5451	8.3917
final component values: co-simulation	stage 1	24	10	16	8
	stage 2	12	8	9.5	8

the two-stage APN with negative slope linear group delay response designed in Section 2.3 for $f = 0.5$ to 1 GHz is implemented using commercially available SMD components on a printed circuit board.

Given the design parameters N, $\{\omega_{r1}, \omega_{r2}, \dots, \omega_{rN}\}$ and $\{k_1, k_2, \dots, k_N\}$, a network topology is chosen for the individual APN stages. The different network realisations and canonical forms of APN are given in [27, 30]. Since at RF, the component values may become unrealisable for low values of k, different network transformations have to be applied [28]. An unbalanced bridged T circuit for $k < 1$ is chosen for implementation and the two-stage cascaded circuit topology is shown in Fig. 1b. The individual component values are obtained from the design formulas in [27, 30] and are tabulated in Table 5. Board level implementation of APN degrades the S-parameters performance from ideal component design. The individual circuit components have to be rounded off to the nearest commercially available component values. The transmission line pads for SMD mounting introduces parasitic of the order of component values and have to be further tuned to nullify the parasitic effect and terminating impedance matching for all stages. The co-simulation design steps to transform the multi-stage APNs to final hardware prototype is shown in Fig. 1b.

The $S21$ becomes notably different with component value round off. Adjusting the component values and pad dimensions is the key to achieve the specified response with low-loss characteristics. The final component values for the modified two-stage design are also tabulated in Table 5. The variation of S-parameters from ideal design to co-simulation design for a negative slope group delay APN is shown in Fig. 6. The group delay of the co-simulation design is within $\pm 7\%$ variation from the specified group delay response. The $S11$ is better than -15 dB and $S21$ is better than -0.43 dB over the bandwidth.

The inductors and capacitors used in the co-simulation procedure above are ideal, having extremely high Q, of the order of 1000.
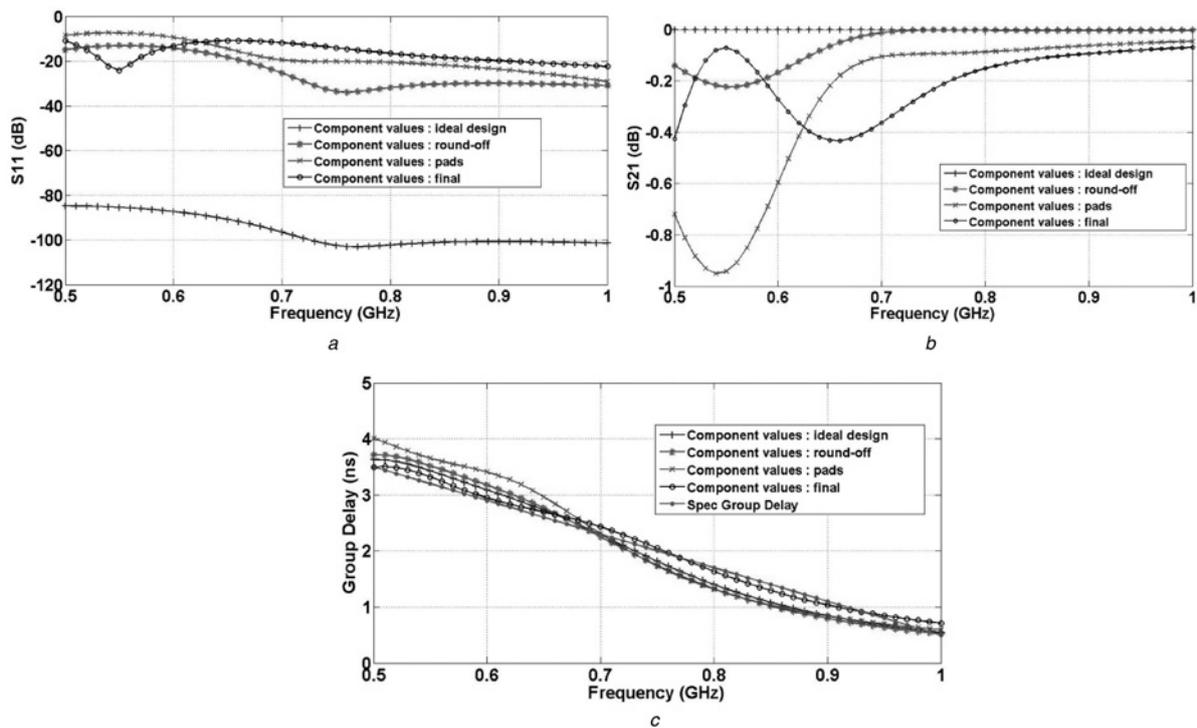
Table 4 Design parameters of multi-stage APN for different ε_{spec}

Stage no.		1	2	3	4	5	6	7	8
design 1 $\varepsilon_{spec} = 0.01$	f_r, GHz	5.1	4.65	4.13	3.6	3.05	2.5	1.85	1.155
	k	0.135	0.201	0.263	0.35	0.45	0.55	0.695	0.932
design 2 $\varepsilon_{spec} = 0.06$	f_r, GHz	5.01	4.3	3.45	2.46	1.365			
	k	0.14408	0.21008	0.31368	0.47724	0.93			

Fig. 6 *Evolution of performance parameters from an ideal component design to a co-simulation design*

a S11
b S21
c Group delay

However, commercially available SMD components have limited range of *Q* values. Typically commercial SMD inductors have a *Q* factor in the range of 50–100 whereas the capacitors have relatively high *Q* of the order of 500. For board and chip level implementations, the realised *Q* of components are often lower.

A systematic analysis is carried out for different values of component *Q*, ranging from 5 to 200. A value of 5 is chosen, comparable to the *Q* that can be achieved with distributed components on an RF substrate. It can be observed from Fig. 7 that change in *Q* affects only the loss characteristics, whereas the group delay response remains almost the same. The lower the value of *Q*, higher will be the dissipation in the circuit and thereby higher loss.

The above results show that the *Q* factor has a negligible effect on the group delay response in the operational frequency band.
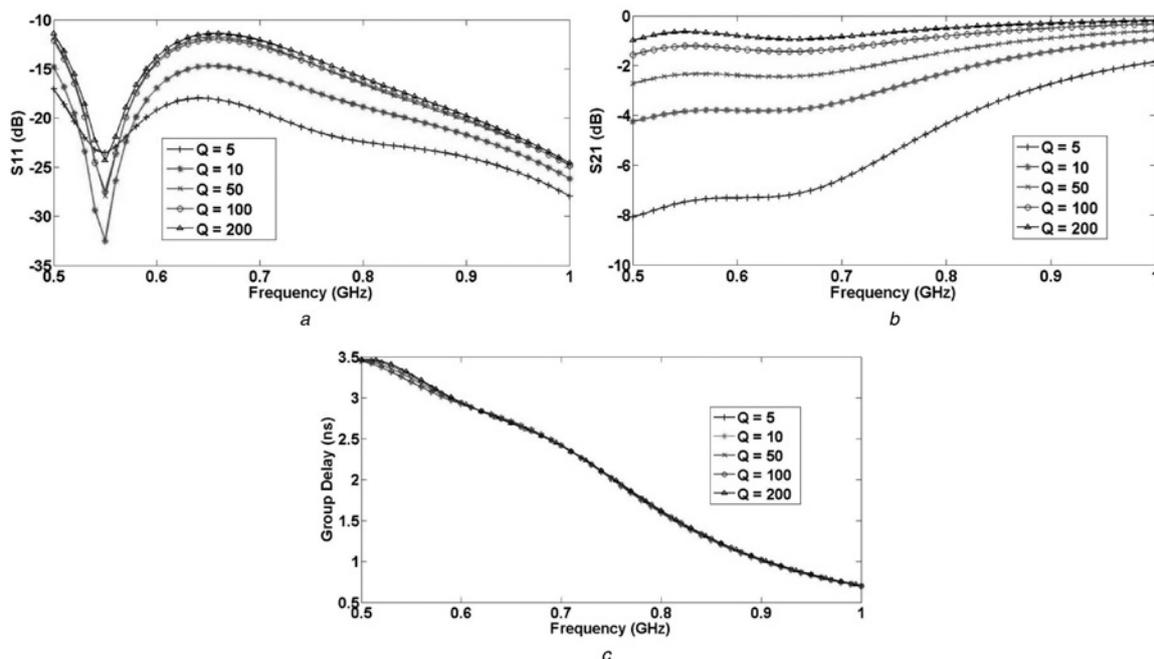

Fig. 7 *Effect of component Q on the performance of two-stage APN implementation*

a S11
b S21
c Group delay

Table 6 Component details of the two stage design for negative slope linear group delay response

	Final component values	Q at f_{res}(MHz)	Model number	Vendor
L_{a1}	24 nH	51 at 900	744 765 124 A	WurthElectronics, Niedernhall, Germany
L_{b1}	16 nH	54 at 900	744 765 116 A	
L_{a2}	12 nH	51 at 900	744 765 112 A	
L_{b2}	9.5 nH	45 at 900	744 765 095 A	
C_{a1}	10 pF	600 at 800	CBR04C 100 F5 GAC	KemetCorporation, Simpsonville, South Carolina
C_{b1}	8 pF	560 at 800	CBR04C 089 B1 GAC	
C_{a2}	8 pF	560 at 800	CBR04C 089 B1 GAC	
C_{b2}	8 pF	560 at 800	CBR04C 089 B1 GAC	

Fig. 8 *Photograph of the fabricated hardware*

components used are tabulated in Table 6. A photograph of the developed hardware is shown in Fig. 8.

The circuit is characterised using vector network analyser PNA-N5230A from Keysight Technologies. The measured S-parameters and group delay response of the circuit is shown in Fig. 9. The S21 performance follows the phasing loss effect, where the amount of dissipation is proportional to the time the signal travels in the system [9]. The effect can be observed both in simulation and measurement in Fig. 9b.

Lumped RF circuit design for GDD developed in the paper is compared with various distributed implementations for their performance parameters in Table 7. The present approach has greatly improved the performance in terms of group delay slope with a reduced device footprint and a lower insertion loss. Although the bandwidth achieved using the present two-stage APN implementation is lower than the distributed implementations, this can be improved by increasing the number of stages of APN as shown in Section 2.5. It has also been shown in Fig. 7 that the component Q factor does not affect the group delay response. Therefore, MMIC or LTCC implementations can be employed to improve compactness with minimum parasitics and easy extension to multi-stage. Other possible solution is to implement multiple designs operating in adjacent frequency bands which can be delayed and combined at the output to achieve full band characteristics [10].
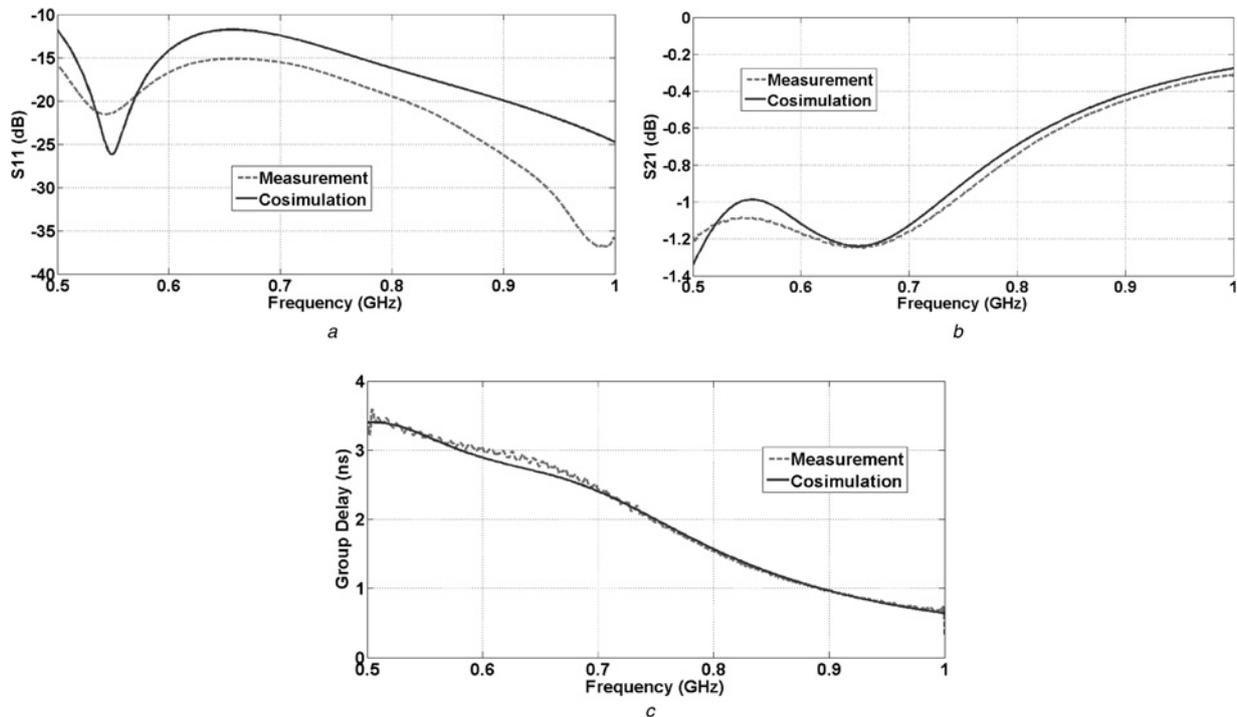
Therefore, the APN circuit can even be implemented in other technologies such as monolithic microwave integrated circuit (MMIC) and low temperature cofired ceramic (LTCC). The co-simulation procedure and implementation in this section using SMD components is for proof of concept. It is to analyse and establish the challenges of the lumped component design.

4 Hardware measurement and discussion

The circuit obtained by two-stage co-simulation design in Section 3 is fabricated on Arlon AD250 with $\varepsilon_r = 2.5$. The details of the

Fig. 9 *Co-simulation and measurement comparison of the fabricated circuit*
a S11
b S21
c Group delay

Table 7 Comparison of distributed and lumped implementation for GDD control

Technology	Frequency band, GHz	Slope, ns/GHz	Device footprint	Insertion loss loss, dB
stripline with chirped EBG [17]	[2–10]	−0.5	28 cm (length)	~7
distributed C-section: edge coupled [12]	[1–5]	+0.32	18 mm × 16.5 mm	~7
distributed C-section: broadside coupled [21]	[6–10]	−0.215	12.5 mm × 14.9 mm	~6
lumped SMD design two-stage APN	[0.5–1]	−6	6 mm × 6.8 mm	1.2

5 Conclusions

Circuits and components with a control on the GDD have multiple applications at broadband RFs but very few implementations are available. Many of these suffer from high insertion loss and are bulky, especially for low RF and high GDD. In this paper, an iterative design procedure is developed to achieve a monotonous group delay response over a broad bandwidth. The approach facilitates cascading of multiple stages of lumped APN with different ω_r and k to obtain required linear and non-linear group delay responses with both positive and negative slopes. Cascading of APNs with same ω_r is shown to increase the GDD over a fixed bandwidth. The design also makes the device footprint independent of the frequency, limited only by the Q factor of the adopted technology.

The ideal component design is further extended using ADS co-simulation for SMD implementation to accommodate mounting pads, component availability, tolerance and finite Q factor. A two-stage APN with negative slope linear group delay response is designed and implemented using commercially available SMD components. The realised circuit shows a group delay slope of −6 ns/GHz in 500 MHz–1 GHz frequency band. The performance parameters of the final realisation are found to be significantly better than past approaches in terms of GDD, insertion loss and device footprint. The circuit may find applications in spectrum sensing and frequency discrimination for cognitive radio.

6 References

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