An Ultrawideband CMOS Low-Noise Amplifier for 3.1–10.6-GHz Wireless Receivers

Andrea Bevilacqua, *Student Member, IEEE,* and Ali M. Niknejad, *Member, IEEE*

***Abstract*—An ultrawideband 3.1–10.6-GHz low-noise amplifier employing an input three-section band-pass Chebyshev filter is presented. Fabricated in a 0.18-μm CMOS process, the IC prototype achieves a power gain of 9.3 dB with an input match of −10 dB over the band, a minimum noise figure of 4 dB, and an IIP3 of −6.7 dBm while consuming 9 mW.**

***Index Terms*—Chebyshev filter, CMOS, low-noise amplifier (LNA), low power, RFIC, ultrawideband (UWB).**

I. Introduction

ULTRAWIDEBAND (UWB) systems are a new wireless technology capable of transmitting data over a wide spectrum of frequency bands with very low power and high data rates. Among the possible applications, UWB technology may be used for imaging systems, vehicular and ground-penetrating radars, and communication systems. In particular, it is envisioned to replace almost every cable at home or in an office with a wireless connection that features hundreds of megabits of data per second [1].

Although the UWB standard (IEEE 802.15.3a [2]) has not been completely defined, most of the proposed applications are allowed to transmit in a band between 3.1–10.6 GHz. Two possible approaches have emerged to exploit the allocated spectrum. One is a multiband approach, with fourteen 500-MHz subbands, OFDM modulation and, possibly, a frequency-hopping scheme [3]. Another possibility is the so-called "impulse radio" [4], based on the transmission of very short pulses, with pulse position or polarity modulation.

In many ways, UWB benefits from existing wireless techniques and standards, as modulation schemes, multiple-access techniques, and transmitter/receiver architectures are adapted for UWB.

A UWB receiver, diagrammed in Fig. 1, will feature a low-noise amplifier (LNA) followed by a correlator that removes the carrier (or the pseudocarrier) from the received radio frequency (RF) signal. Analog-to-digital conversion will then allow for digital signal processing aimed at recovering the information data. In this context, it is clear that, regardless of what the future standard will be, a wideband LNA operating over the entire 7.5-GHz band of operation is required. Such an amplifier must feature wideband input matching to a 50-Ω antenna for noise optimization and filtering of out-of-band interferers. Moreover, it must show flat gain over the entire bandwidth, good linearity, minimum possible noise figure (NF) and low power consumption.

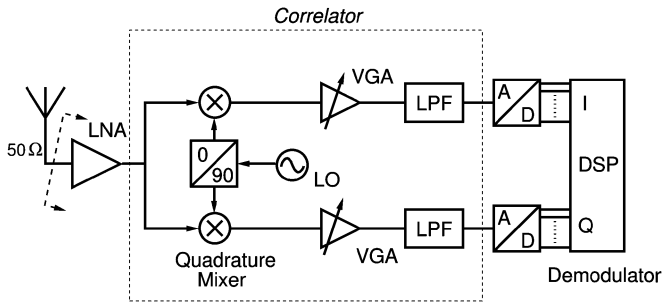

Fig. 1. Block diagram of a UWB receiver. The dashed box represents the subsystem that brings the RF signal to baseband in order to recover the information signal: it can be a correlation filter followed by a sampler or, as depicted here as an example, a quadrature mixer.

This paper focuses on the design and implementation of a low-noise amplifier (LNA) in a 0.18-μm CMOS technology for the receiver path of a UWB system. The paper is organized as follows. In Section II, the issues related to the design of a wideband LNA are summarized, and the approach employed in this work is discussed. In Section III, the proposed circuit is analyzed, and the circuit design issues are discussed in Section IV. Experiments carried out on the fabricated LNA prototypes are reported in Section V.

II. Design Challenges

Designing wideband LNAs for wireless applications presents two levels of challenges. In the first place, having fast and low-noise transistors depends on the available technology. Traditionally, wideband microwave amplifiers relied on transistors realized with composite semiconductors, e.g., GaAs, because of the intrinsic superior frequency characteristics of such devices [5]–[7]. Silicon technology, on the other hand, has been employed to design and fabricate amplifiers, even wideband ones, for particular applications, e.g., optical communications [8], [9], that require different specifications compared to wireless systems. In wireless mobile communications systems, silicon integrated circuits have been widely employed in narrow-band systems, where limited gain and increased parasitics are tolerable due to lower operating frequencies and the application of tuned networks.

There are few examples of development of high-frequency wideband amplifiers employing silicon transistors, in particular

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A. Bevilacqua is with the Dipartimento di Ingegneria dell'Informazione, Università di Padova, 35131 Padova, Italy (e-mail: andrea.bevilacqua@dei.unipd.it).

A. M. Niknejad is with the Berkeley Wireless Research Center, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA.

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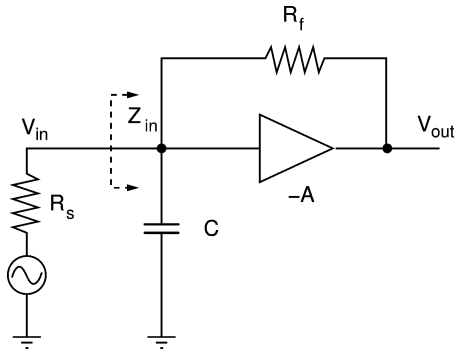

Fig. 2. Conceptual schematic of a shunt feedback amplifier.

in CMOS technology. In this case, it is remarkable that employed solutions (distributed amplifiers [10]–[12]) require high levels of power consumption, and they are not optimized for noise. This brings about the second challenge—finding a low-power topology that satisfies all the other design requirements, the most stringent one being the input match.

Classic shunt feedback amplifiers have limited input match at higher frequencies due to the parasitic input capacitance. In Fig. 2 a conceptual schematic of a shunt feedback amplifier is shown. The input impedance is $Z_{\rm in}(s) = R_s/(1 + sR_sC)$, where the gain A is chosen such that $R_f/(1 + A) = R_s$. As a consequence, the maximum input capacitance that can be tolerated to achieve an input reflection coefficient equal to $|\Gamma| = -10$ dB at $f = 10$ GHz is as low as $C = (1/\pi R_s f)\sqrt{|\Gamma|^2/(1-|\Gamma|^2)} = 200$ fF. Satisfying this requirement with a CMOS amplifier stage while achieving sufficient gain and low noise is difficult. This issue is solved by distributed amplifiers, but at the cost of a power consumption that is five to ten times higher than in a single-stage amplifier, as previously mentioned.

Another possibility is balanced amplifiers. In this case, though, the input match is achieved by means of a resistive termination. This results in a degradation of the overall noise performance, as the minimum achievable NF is 3 dB. Moreover, balanced amplifiers require quadrature hybrid couplers that are either narrow band or, if they are wideband, they are multisectional and very large. Thus, they are not amenable to integration.

The proposed solution, shown in Fig. 3, expands the use of an inductively degenerated common-source amplifier, a technique widely used in narrow-band designs [13] by embedding the input network of the amplifying device in a multisection reactive network so that the overall input reactance is resonated over a wider bandwidth. A similar technique has enabled narrow-band LNAs to act as multiband concurrent LNAs [14]. In this way, a wideband input match is achieved and, at the same time, good noise performance is attained. In fact, for MOS devices, noise match is very close to power match [13]. To add flexibility to the design, an inductor (L_g) is placed in series with the gate, and a capacitor (C_p) is placed between the gate and the source of the input device. The cascode configuration (M_1 and M_2) improves the input–output reverse isolation and the frequency response of the amplifier. The source-follower buffer (M_3) is intended for measurement purposes, namely to drive an external 50-Ω load. The proposed topology is analyzed in Section III.

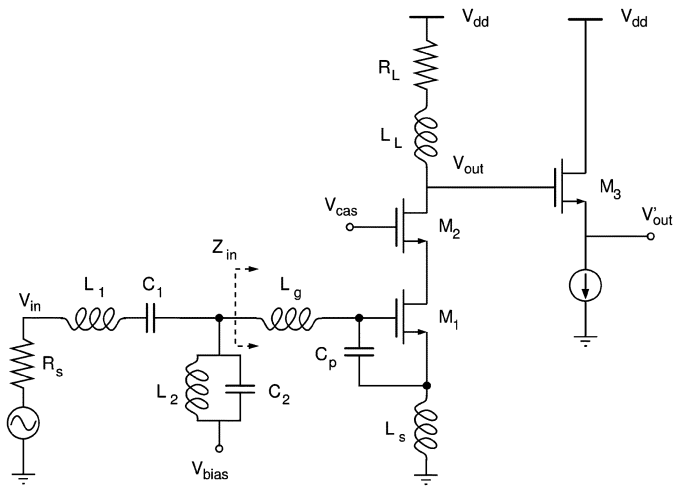

Fig. 3. Simplified schematic of a wideband LNA.

III. Circuit Analysis

The use of inductive local series feedback allows the synthesis of a specified real part for the input impedance equal to $\omega_T L_s$ in a broadband fashion, where ω_T is the cutoff frequency of the transistor. In a narrow-band design, the reactive part of the input impedance is resonated at the carrier frequency. This yields nearly optimal NF at that frequency [13]. In the proposed wideband design, shown in Fig. 3, a doubly terminated three-section passband Chebyshev filter structure is used to resonate the reactive part of the input impedance over the whole band from 3.1 to 10.6 GHz.

A. Input Match

The input impedance of the MOS transistor with inductive source degeneration is a series RLC circuit

$$\begin{aligned} Z_{\rm in}(s) &= \frac{1}{s(C_{\rm gs}+C_p)} + s(L_s+L_g) + \omega_T L_s \\ &= \frac{s^2(L_s+L_g)(C_{\rm gs}+C_p) + s\omega_T L_s(C_{\rm gs}+C_p)+1}{s(C_{\rm gs}+C_p)} \end{aligned} \tag{1}$$

where $\omega_T = g_m/(C_{\rm gs}+C_p) = g_m/C_t$. This network is embedded in the Chebyshev filter structure. A T-network topology is chosen, as shown in Fig. 4. The real part of $Z_{\rm in}$ is ideally chosen to be equal to the source resistance (filter termination), that is, $\omega_T L_s = R_s$. In the filter passband, the power loss is 0 dB, with a ripple ρ_p. The choice of reactive elements in the filter determines the bandwidth and the in-band ripple. The input reflection coefficient Γ is related to ρ_p by

$$|\Gamma|^2 = 1 - \frac{1}{\rho_p}. \tag{2}$$

The picture described so far is complicated by the presence of the gate–drain capacitance of M_1 $(C_{\rm gd})$. The real part of $Z_{\rm in}$

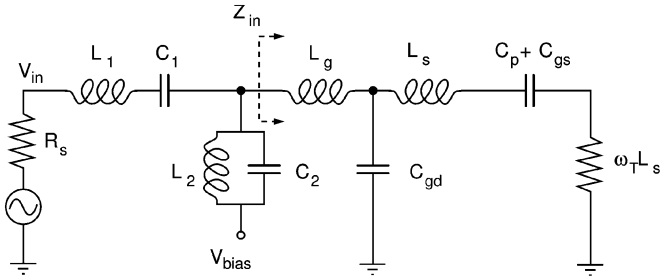

Fig. 4. Schematic of the LNA input network.

is decreased with respect to (1). The desired branch series resonance is determined by the resonance of L_g and the parallel combination of $C_{\rm gd}$ and the equivalent capacitance due to the series combination of L_s and C_t, i.e., $C_t/(1-\omega^2 L_s C_t)$. $C_{\rm gd}$ also introduces one more parallel resonance and one more series resonance with respect to (1). The parallel resonance essentially occurs between L_s and $C_{\rm gd}$. The second series resonance, on the other hand, occurs between L_g and the equivalent capacitance resulting from the parallel combination of L_s and $C_{\rm gd}$ at frequencies higher than the parallel resonance.

B. Gain Analysis

To derive the voltage gain of the proposed amplifier, notice that the input network impedance is equal to $R_s/W(s)$, where $W(s)$ is the Chebyshev filter transfer function. Note that $|W(s)|$ is approximately unity in-band and tends to zero out-of-band. The impedance looking into the amplifier is therefore equal to R_s in-band, and it is very high out-of-band. The current flowing into M_1 is $v_{\rm in}\cdot W(s)/R_s$. At high frequency, the MOS transistor acts as a current amplifier, the current gain being $\beta(s)=g_m/(sC_t)$. As a consequence, the output current is, assuming ideal cascode operation, $v_{\rm in}\cdot W(s) g_m/(sC_tR_s)$. The load is a shunt-peaking resistor [13]. The overall gain is therefore

$$\frac{v_{\rm out}}{v_{\rm in}}=-\frac{g_m W(s)}{sC_tR_s}\cdot\frac{R_L\left(1+\dfrac{sL_L}{R_L}\right)}{1+sR_LC_{\rm out}+s^2L_LC_{\rm out}} \tag{3}$$

where R_L is the load resistance, L_L is the load inductance, and $C_{\rm out}$ is the total capacitance between the drain of M_2 and ground, i.e., $C_{\rm out}=C_{\rm db2}+C_{\rm gd3}$, where $C_{\rm db2}$ is the drain–bulk capacitance of M_2 and $C_{\rm gd3}$ is the gate–drain capacitance of M_3. Equation (3) shows that the current gain roll-off is compensated by L_L. Moreover, it shows that $C_{\rm out}$ introduces a spurious resonance with L_L, which must be kept out-of-band.

The parasitic capacitances at the source and drain nodes of M_1 have a detrimental effect on the amplifier performance. The source–bulk capacitance of M_1 ($C_{\rm sb1}$) shunts L_s, as shown in Fig. 5(a). If the resulting parallel resonance is in-band, the inductive source degeneration is compromised. On the other hand, at lower frequencies, the inductance is boosted. The result is an undesirable frequency dependence in the synthesized real part of the input impedance. The total parasitic capacitance at the drain of M_1 (sum of $C_{\rm db1}$, and $C_{\rm gs2}$) introduces a pole that limits the bandwidth of the amplifier at high frequencies.

The performance of the amplifier is improved by connecting the bulk of M_1 to its source. In this way, $C_{\rm sb1}$ is shorted, while

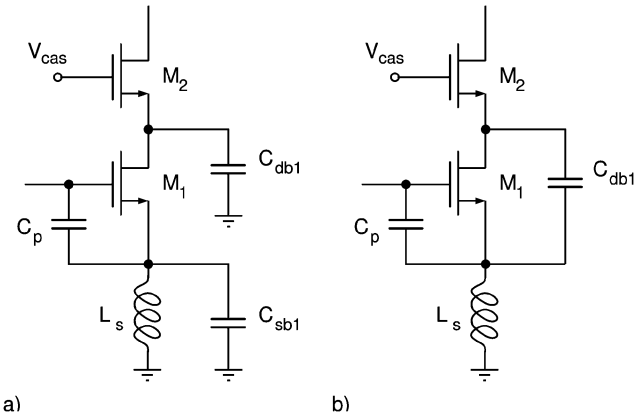

Fig. 5. Impact of parasitic capacitances. The bulk is (a) grounded and (b) connected to the source.

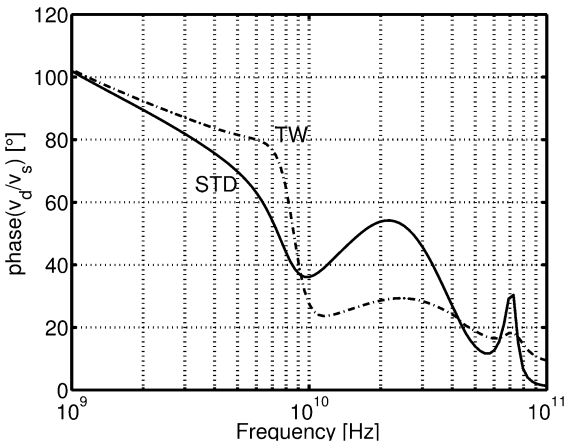

Fig. 6. Phase of the drain–source gain for the case of grounded bulk (solid line) and of bulk connected to the source of M_1 (dash–dotted line).

$C_{\rm db1}$ is connected between the drain and the source of M_1, as illustrated by Fig. 5(b). In order to assess the advantage of this configuration, we compute the voltage gain between the drain and the source nodes. As previously noted, in-band, the input current is equal to $v_{\rm in}/R_s$. The current flowing through L_s is $v_{\rm in}/R_s\cdot[1+\beta(s)]$, and the source voltage is $v_s=v_{\rm in}/R_s\cdot[1+g_m/(sC_t)]sL_s$. The voltage at the drain is equal to $v_d=-v_{\rm in}/R_s\cdot g_m/[sC_t(g_{m2}+sC_x)]$, where C_x is the total capacitance at the drain node. The drain–source voltage gain is thus

$$\frac{v_d}{v_s}=-\frac{1}{\left(1+\dfrac{sC_t}{g_m}\right)\left(1+\dfrac{sC_x}{g_{m2}}\right)sL_sg_{m2}}. \tag{4}$$

Equation (4) shows that the phase of the drain–source gain decreases from 90° at low frequencies to −90° at high frequencies. Both the two high-frequency poles are expected to be out-of-band. The phase of v_d/v_s is expected to be around 90° at the lower edge of the band and to decrease to around 0° at the upper edge of the band. As a consequence, due to the Miller effect, the contribution of $C_{\rm db1}$ to C_x at higher frequencies is very small. This results in an enhancement of the bandwidth of the amplifier. This intuitive and very simplified picture is confirmed by the simulation showed in Fig. 6 where the phase of v_d/v_s is shown. Note that, at higher frequencies, the presence of other

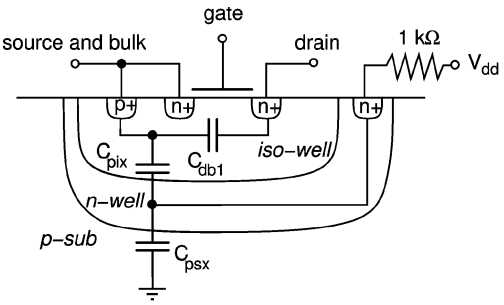

Fig. 7. Cross section of a triple-well device.

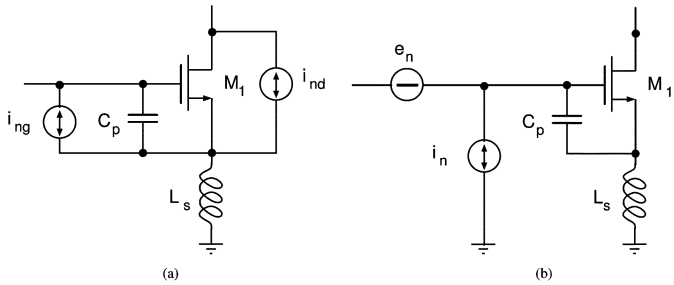

Fig. 8. Noise model for the amplifying transistor M_1. (a) M_1 noise sources. (b) Input-referred equivalent noise generators.

zeros and poles due to circuit elements neglected in the foregoing analysis.

In order to connect the bulk terminal to the source terminal, the application of triple-well devices has been explored. However, triple-well devices introduce extra parasitics, as illustrated in Fig. 7. In fact, the bulk terminal tends to be shunted to ground by the parasitic capacitance between the isolated well and the n-well ($C_{\rm pix}$), as the n-well must be connected to $V_{\rm dd}$ to avoid latch-up. We make use of a 1-kΩ isolation resistor. Consequently, the path from the bulk terminal to ground is made up of the series combination of $C_{\rm pix}$ and the parasitic junction capacitance between the n-well and the p-substrate, $C_{\rm psx}$. Since $C_{\rm psx} < C_{\rm pix}$, this new path is at higher impedance. For the process considered in this design, $C_{\rm psx} \approx C_{\rm pix}/4$. The series combination of $C_{\rm pix}$ and $C_{\rm psx}$ is thus five times smaller than $C_{\rm pix}$ alone.

The source-follower buffer (M_3 in Fig. 3) is needed to drive an external low-impedance load, i.e., it is required to improve the power gain of the amplifier. The external output voltage $v'_{\rm out}$ is related to the output voltage of the amplifier by

$$\frac{v'_{\rm out}}{v_{\rm out}} = \frac{g_{m3}R_{\rm ext}}{1+g_{m3}R_{\rm ext}} \tag{5}$$

where $R_{\rm ext}$ is the external load resistance, i.e., 50 Ω.

C. Noise Analysis

The noise performance of the proposed topology is determined by two main contributors: the losses of the input network and the noise of the amplifying device M_1. The noise contribution of the input network is due to the limited quality factor Q of the integrated inductors. Its optimization relies on achieving the highest Q for a given inductance value. The optimization of the noise contribution from M_1 relies instead on the choice of its width for a given bias current. Optimum device width has been fully discussed in the literature in the case of narrow-band LNA design [13]. We extend the analysis to the wideband case, i.e., we investigate the amplifier noise behavior over a wide range of frequencies. Optimization is performed on the in-band average NF, as opposed to the spot NF (i.e., NF at a single frequency), used in the narrow-band case.

The analysis follows the guidelines of [13] in a dual fashion and with the difference that the loading effect of the local feedback inductor is taken into account. MOS transistor noise sources, shown in Fig. 8(a), are input-referred in a conventional way and replaced with two correlated noise generators, as shown in Fig. 8(b):

$$i_n = i_{\rm ng} + \frac{j\omega C_t}{g_m} i_{\rm nd} \tag{6}$$

$$e_n = j\omega L_s i_{\rm ng} + \left(1-\omega^2 C_t L_s\right)\frac{i_{\rm nd}}{g_m} = \frac{i_{\rm nd}}{g_m} + j\omega L_s i_n \tag{7}$$

where $i_{\rm nd}$ is the drain noise current, due to the carrier thermal agitation in the channel, while $i_{\rm ng}$ is the induced gate noise, due to the coupling of the fluctuating channel charge into the gate terminal. The induced gate noise and drain current noise power spectral densities are, respectively [13]

$$S_{i_{\rm ng}}(\omega) = 4kT\delta\frac{\omega^2 C_{\rm gs}^2}{5g_{d0}} \tag{8}$$

$$S_{i_{\rm nd}}(\omega) = 4kT\gamma g_{d0} \tag{9}$$

where $\delta \approx$1.33–4, and $\gamma \approx$0.67–1.33 are excess noise parameters [15], and g_{d0} is the channel conductance at $V_{\rm DS} = 0$.

The noise voltage e_n can be expressed as the sum of two components, one fully correlated, $e_{\rm nc}$, and the other, $e_{\rm nu}$, uncorrelated to the noise current i_n as follows:

$$e_n = e_{\rm nc} + e_{\rm nu}. \tag{10}$$

Carrying out the calculations, the correlation impedance Z_c is written as

$$\begin{aligned} Z_c &= \frac{S_{e_n i_n}(\omega)}{S_{i_n}(\omega)} \\ &= R_c + jX_c \\ &= jX_c \\ &= \frac{1-\omega^2 L_s C_t \cdot \dfrac{1+2|c|p\alpha\chi+p^2\alpha^2\chi^2}{1+|c|p\alpha\chi}}{j\omega C_t \cdot \dfrac{1+2|c|p\alpha\chi+p^2\alpha^2\chi^2}{1+|c|p\alpha\chi}} \end{aligned} \tag{11}$$

where $p = C_{\rm gs}/C_t$, $\chi = \sqrt{\delta/(5\gamma)}$, and $c = S_{i_{\rm ng}i_{\rm nd}}(\omega)/\sqrt{S_{i_{\rm ng}}(\omega)S_{i_{\rm nd}}(\omega)}$ is the correlation coefficient between the gain noise and the drain noise. For MOS devices, the value of c is $\approx\ j0.4$ [15]. The parameter $\alpha = g_m/g_{d0}$ accounts for short-channel effects. It describes the transconductance reduction due to velocity saturation and mobility decrease due to vertical fields [13], [16].

The two uncorrelated noise sources, $e_{\rm nu}$ and i_n, are described by means of the following parameters:

$$R_u = \frac{S_{e_{\rm nu}}(\omega)}{4kT} = \frac{\gamma}{\alpha^2 g_{d0}} \cdot \frac{p^2\alpha^2\chi^2(1-|c|^2)}{1+2|c|p\alpha\chi+p^2\alpha^2\chi^2} \quad (12)$$

$$G_n = \frac{S_{i_n}(\omega)}{4kT} = \frac{\gamma}{\alpha^2 g_{d0}} \cdot \omega^2 C_t^2 (1+2|c|p\alpha\chi+p^2\alpha^2\chi^2) \quad (13)$$

respectively.

By using the introduced parameters, the NF can be expressed by

$$F = 1 + \frac{R_u + |Z_c + Z_s|^2 G_n}{R_s} \quad (14)$$

where $Z_s = R_s + jX_s$ is the source impedance.

Classic noise optimization theory [13], [17] shows that the minimum NF is achieved if the source impedance $Z_s = Z_{\rm opt} = R_{\rm opt} + jX_{\rm opt}$ is chosen such that

$$R_{\rm opt} = \sqrt{\frac{R_u}{G_n} + R_c^2} = \sqrt{\frac{R_u}{G_n}} = \frac{p\alpha\chi\sqrt{1-|c|^2}}{\omega C_t(1+2|c|p\alpha\chi+p^2\alpha^2\chi^2)} \quad (15)$$

where, in our case $R_c = 0$, and

$$X_{\rm opt} = -X_c. \quad (16)$$

Equations (11) and (16) show that the optimum source impedance is roughly the one that resonates the series combination of C_t and L_s. As a consequence, nearly minimum NF is achieved over the entire amplifier bandwidth by using the proposed input network, which produces $X_{\rm opt}$ over a wide bandwidth. As a result of the foregoing discussion, the NF of the LNA is

$$F(\omega) \approx 1 + \frac{R_u}{R_s} + G_n R_s = 1 + \frac{P(\omega)}{g_m R_s} \cdot \frac{\gamma}{\alpha} \quad (17)$$

where

$$P(\omega) = \frac{p^2\alpha^2\chi^2(1-|c|^2)}{1+2|c|p\alpha\chi+p^2\alpha^2\chi^2} + \omega^2 C_t^2 R_s^2 (1+2|c|p\alpha\chi+p^2\alpha^2\chi^2). \quad (18)$$

Equations (17) and (18) show that, as $p \leq 1$, $\alpha \leq 1$, and, typically, $\chi < 1$, using a smaller transistor for a given g_m, i.e., drawing more current, is preferable. Moreover, they show that increasing the transconductance improves the noise performance, with all of the other parameters being the same.

The LNA NF described by (17) depends on three of the following four quantities: the drain bias current I_D, the over-drive voltage $V_{\rm od}$, the transistor width W, and the frequency. In order to perform an optimization over the entire band of interest, we consider the average NF. Thus, we reduce the number of independent variables by one. Fig. 9 shows the contour plots of the average NF as a function of I_D and W. For each value of the bias current, the device width can be chosen to minimize the NF. In particular, for I_D =5 mA, the best noise performance is achieved if $250 < W <$450 μm. Note that the quantitative results of Fig. 9 only refer to the noise contribution of M_1. The NF in an actual LNA implementation is thus expected to be worse because of:

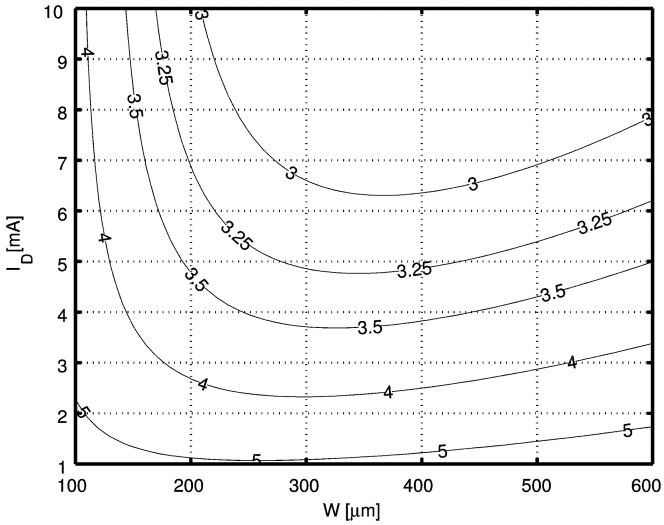

Fig. 9. Contour plots of the average NF $\rm NF_{avg}$.

- the losses of the input network, i.e., the limited quality factor of the integrated inductors;
- the cascode device (M_2) noise contribution, particularly significant at higher frequencies;
- the load resistance (R_L) noise contribution;
- the output buffer (M_3) noise contribution.

Nonetheless, Fig. 9 gives important insights, as it shows that the noise optimization of the wideband design follows the same guidelines as the narrow-band counterpart. For a given current budget, there is a value of W that yields the best average NF. If better noise performance is required, the design can be improved by raising the bias current, as long as the noise performance is limited by the contribution of M_1. Moreover, note that the NF decreases with the scaling of MOS technology.

Fig. 10(a) reports the simulated noise contributions $(F-1)$ due to M_1 only (solid line), to the losses of the input network (dashed line), and to the cascode device M_2, the load, and the buffer (dash–dotted line) for the design detailed in Section IV. Note that the main noise contributor is M_1. In Fig. 10(b), the NF is dissected and shown as the noise of M_1 only (solid line), by the sum of the noise of M_1 and the noise of the three-section input network (dashed line), and by the noise of all the contributors in the circuit (dash–dotted line). Again, the dominant role of M_1 is clearly illustrated.

IV. Circuit Design

The first step in the design is the choice of the input network structure. Given a target input reflection coefficient smaller than $-$10 dB in-band, (2) yields a ripple $\rho_p <$0.46 dB. Values for the normalized components of a filter with such a ripple are found in [18] for several filter prototypes. The components of the actual

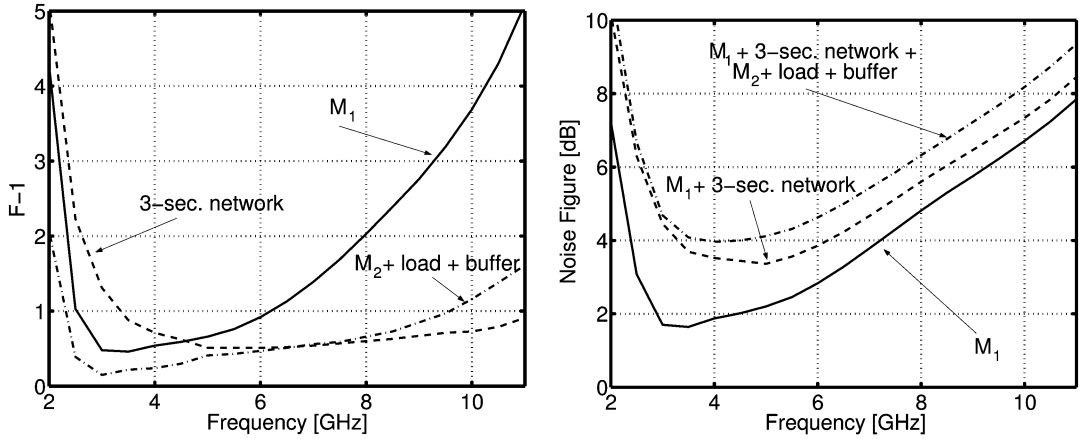

Fig. 10. Noise contributors of the designed LNA. (a) Noise contributions due to M_1 (solid line), input network (dashed line), and M_2, load and M_3 (dash–dotted line). (b) NF set by M_1 only (solid line), by M_1 and input network (dashed line), and by all circuit components (dash–dotted line).

TABLE I
INPUT NETWORK COMPONENTS

Type	Sec.	L_1 [nH]	C_1 [fF]	L_2 [nH]	C_2 [fF]	$L_g + L_s$ [nH]	C_t [fF]
Chebyshev	3	1.3	650	1.6	490	1.3	650
Butterworth	2	–	–	2.2	350	0.65	1200

filter are obtained by denormalization, setting the appropriate bandwidth (3.1–10.6 GHz) and center frequency (5.7 GHz). Table I shows the component values for a three-section Chebyshev structure and a two-section maximally flat prototype. The three-section structure is chosen as a compromise between filter complexity and component values. Note that the two-section implementation requires that C_t =1.2 pF. This would require an extremely high g_m to ensure adequate gain, as shown by (3), and noise performance, as shown by (17) and (18).

The width of M_1 (240 μm) is optimized for noise. For a given current budget (5 mA), it is sized so that the contributions of thermal and induced gate noise are balanced. The gate–drain capacitance of M_1 makes the input impedance $Z_{\rm in}$ differ from a simple series RLC model. The real part is decreased compared to $g_m L_s/C_t$, as discussed in Section III-A, so that the source inductance must be set to $L_s > R_s C_t/g_m$. The series resonance of $Z_{\rm in}$ is approximately determined by L_g and $C_{\rm gd} + C_t/\left(1-\omega^2 L_s C_t\right)$. As a consequence, L_g is set larger than $L_1 - L_s$. Moreover, C_t must be smaller than $C_1 - C_{\rm gd}$, as the series combination of C_t and L_s boosts the capacitance. Simulation helps in choosing the final values of the components: L_g =1.4 nH, L_s =680 pH, and C_p =100 fF.

The cascode device is chosen to be as small as possible to reduce the parasitic capacitances. A lower limit to the width of M_2 is set by its noise contribution. The selected value for the width of M_2 is 60 μm. Both M_1 and M_2 are minimum length devices (0.18 μm).

The load is designed to achieve flat gain over the whole bandwidth. The choice of L_L is determined by two opposite requirements [see (3)]: L_L must be sizable to have large gain, and it must be small so that it resonates $C_{\rm out}$ out-of-band. R_L is chosen to place the zero frequency ($\omega_z = R_L/L_L$) as close as possible to the lower edge of the band to improve the gain at lower frequencies. An upper limit to R_L is set by the voltage headroom. The values for the components of the load are: L_L =2.6 nH, and $R_L = 90\,\Omega$.

The LNA is biased by means of a current mirror, not shown in Fig. 3 for clarity. M_1 is biased through one ac-ground point of the filter. This eliminates the noisy bias isolation resistor. Using a power supply $V_{\rm dd}$ =1.8 V, the core power consumption is 9 mW.

The buffer must drive a 50-Ω external load. As a consequence, $g_{m3} = 1/R_{\rm ext}$ and the power gain of the LNA is exactly 6 dB lower than the voltage gain of the core amplifier. The buffer is independently biased by means of a current source made up of two transistors in current mirror configuration. The bias current for M_3 is selected to be 5 mA, and the width of M_3 is 60 μm. The transistors used to implement the current source are 100 μm wide. They feature a nonminimum length (0.36 μm) for higher output impedance.

The design has been carried out in two versions: one makes use of standard devices (STD LNA), while the other makes use of triple-well devices (TW LNA).

V. MEASUREMENT RESULTS

Prototypes have been fabricated in a 0.18-μm CMOS process. A microphotograph of the STD LNA is shown in Fig. 11. The layout is very similar in the two versions with the exception of the active devices. Die area including the pads is 1.1 mm^2. DC pads are electrostatic-discharge (ESD) protected, while RF input and output pads are not. Test measurements have been carried out on wafer.

Figs. 12 and 13 show the measured and simulated input and output reflection coefficients, both for the LNA with standard

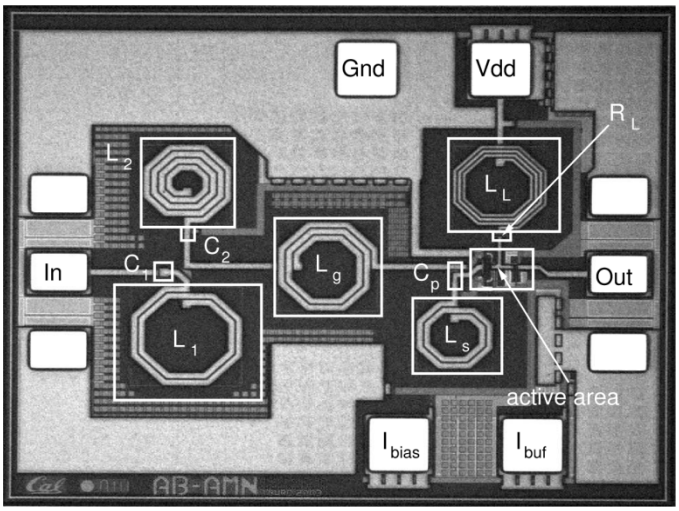

Fig. 11. Microphotograph of the LNA employing standard devices.

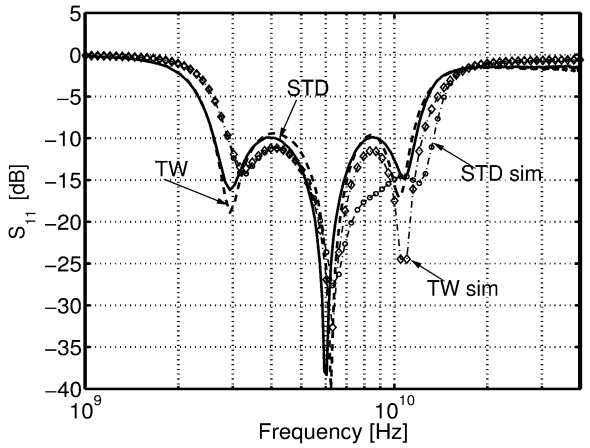

Fig. 12. Measured and simulated input reflection coefficient for STD and TW LNAs.

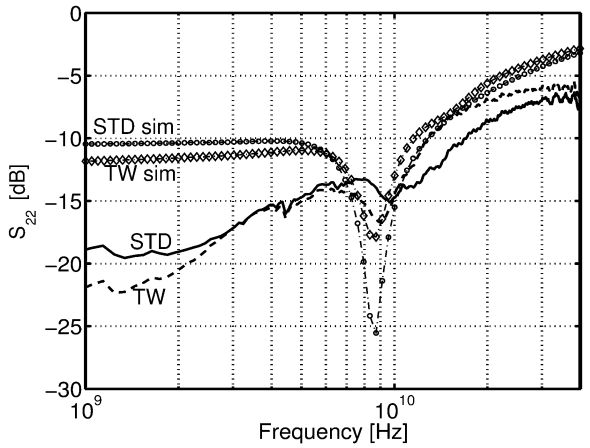

Fig. 13. Measured and simulated output reflection coefficient for STD and TW LNAs.

devices (STD LNA) and the one with triple-well devices (TW LNA). S_{11} is lower than -9.9 dB between 2.6–11.7 GHz for the STD LNA, and lower than -9.4 dB between 2.6–11.5 GHz for the TW LNA. The output buffer achieves excellent matching up to 15 GHz in both cases.

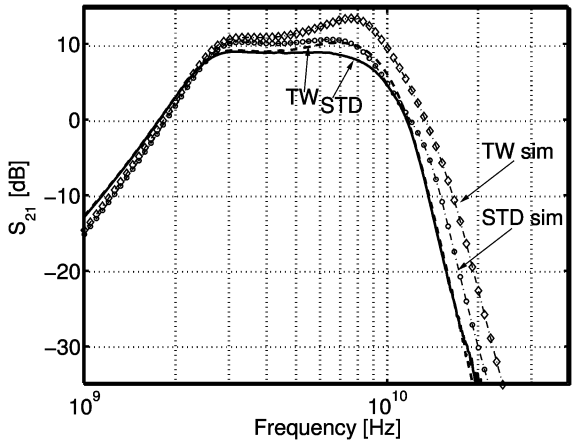

Fig. 14. Measured and simulated power gain for STD and TW LNAs.

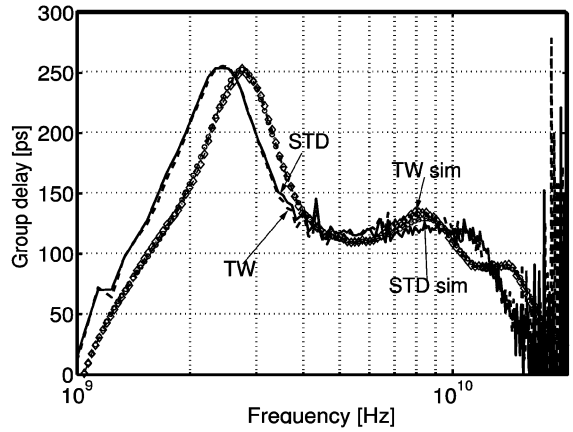

Fig. 15. Measured and simulated group delay for STD and TW LNAs.

In Figs. 14 and 15 the measured and simulated power gain and group delay are reported for both LNAs. The maximum power gain is 9.3 and 10.4 dB for the STD and TW transistors, respectively. Since the output source follower drives a matched load, the voltage gain of the core amplifier is exactly 6 dB higher than S_{21}. The -3-dB bandwidth is 2.3–9.2 GHz for the STD LNA, while the application of the triple-well brings it to 2.4–9.5 GHz. Group delay decreases from 200 to 130 ps for frequencies increasing from 3 to 4 GHz, while it flattens to 120 ps with a 10-ps ripple in the 4–11-GHz range for both amplifiers.

Measured and simulated reverse isolation is depicted in Fig. 16. For the STD LNA, $S_{12} < -43$ dB, demonstrating the effectiveness of the cascode configuration. In the case of the LNA employing triple-well devices, the connection of the drain–bulk parasitic capacitances between drain and source terminals introduces a feedforward path that brings the input–output isolation to be $S_{12} < -35$ dB.

The S-parameters were measured on six different parts for both the STD and the TW LNA. The maximum observed spread of the parameters is less than 1 dB. This result benefits from the use of a ladder-filter input network, a structure well known for its low sensitivity to component variations. It shows, along with the good agreement between measurements and simulation, the robustness of the proposed approach. It is to be noted, though, that, in a production design, packaging parasitics are to be taken

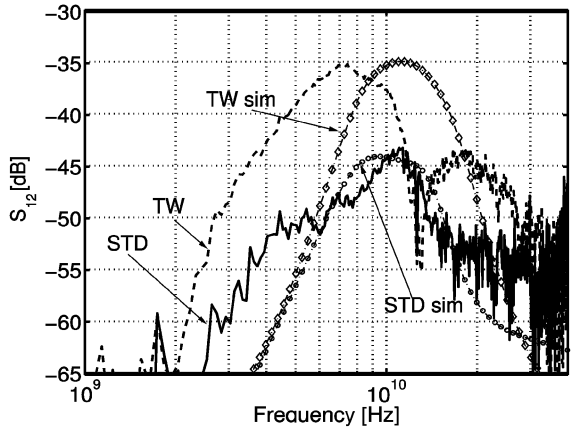

Fig. 16. Measured and simulated reverse isolation for STD and TW LNAs.

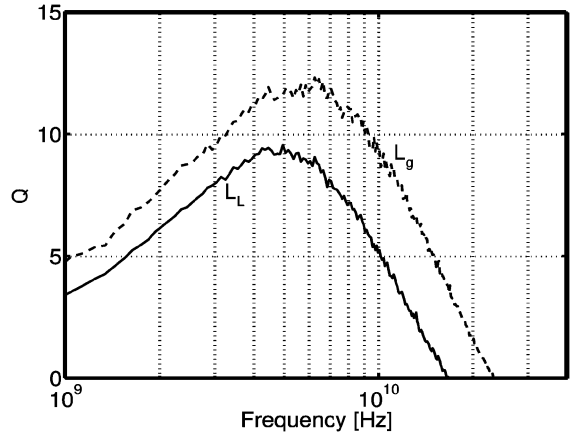

Fig. 17. Measured quality factor for gate and load inductors.

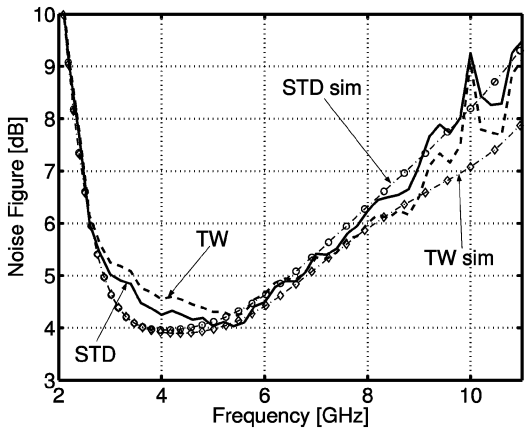

Fig. 18. Measured and simulated spot NF for STD and TW LNAs.

into account in the design of the input network. In a bond-wired solution, inductor L_1 may be implemented as a bond wire whose inductance is, however, quite unpredictable. Another possibility is to implement the entire L_1-C_1 branch externally, so that the pad capacitance is absorbed in C_2, and inductive packaging parasitics add to an external inductor to implement L_1. A preferable solution is to use a bull grid array (BGA) packaging technology. In this case, in fact, the parasitic series inductance is on the order of hundreds of pico-Henry, a quantity comparable to the tolerated component spreads.

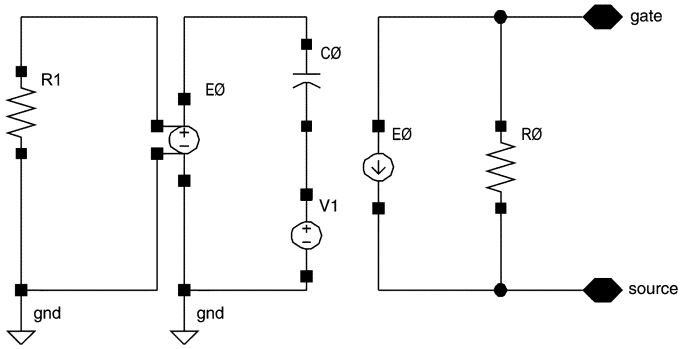

Fig. 19. Circuit model for inclusion of induced gate noise in the simulation.

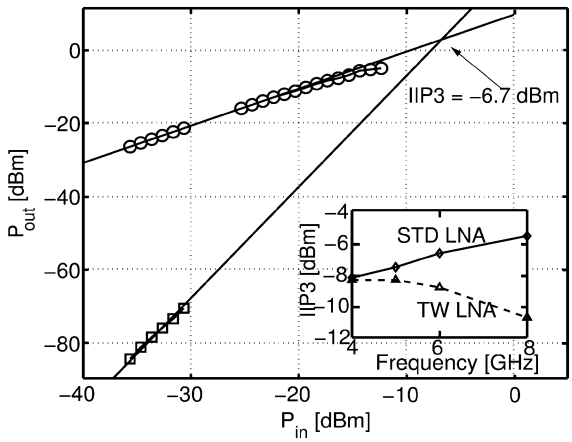

Fig. 20. Measured two-tone test at 6 GHz for STD and TW LNAs. Inset: Measured IIP3 versus frequency.

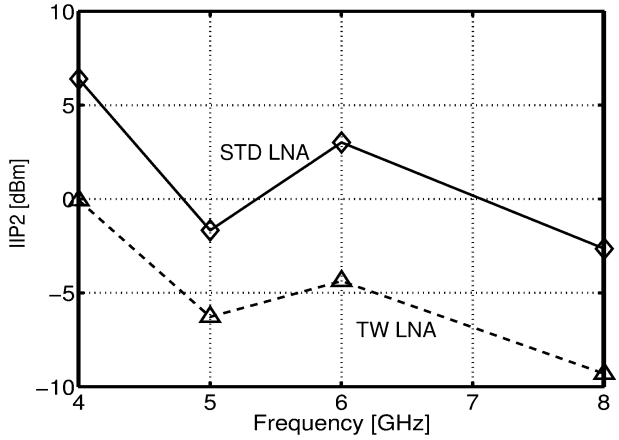

Fig. 21. Measured two-tone IIP2 for STD and TW LNAs.

Two inductors L_g and L_L were included separately as test structures. Their measured quality factor is reported in Fig. 17. In-band, Q is higher than 8 and 6 for L_g and L_L, respectively. L_g features 10-μm-wide traces, versus the 5-μm-wide traces of L_L, accounting for the higher Q. The measured inductance value and self-resonance frequency are 1.5 nH and 23 GHz for L_g and 2.8 nH and 17 GHz for L_L, respectively. Inductor parameter spread over six measured parts is negligible.

The measured NF of the two amplifiers is shown in Fig. 18 along with the simulated results. The minimum NF is as low as 4.0 dB (STD) and 4.2 dB (TW), the STD LNA having a slightly

TABLE II
SUMMARY OF LNA PERFORMANCE, AND COMPARISON WITH PREVIOUSLY PUBLISHED DESIGNS

	Tech.	S_{11} [dB]	$G_{\max}$ [dB]	B [GHz]	$NF_{\min}$ [dB]	$IIP3$ [dBm]	ICP [dBm]	P_{diss} [mW]
STD LNA	0.18 μm CMOS	< -9.9	9.3	2.3–9.2	4.0	-6.7^{*}	-15^{*}	9
TW LNA	0.18 μm CMOS	< -9.4	10.4	2.4–9.5	4.2	-8.8^{*}	-18^{*}	9
[11]	0.18 μm CMOS	< -8	8.1	0.6–22	4.3	N/A	N/A	52
[12]	0.6 μm CMOS	< -7	7.4	0.5–4	5.4	N/A	6–7.5†	83.4
[10]	0.6 μm CMOS	< -6	7	1.5–7.5	8.7	N/A	N/A	216
[20]	0.25 μm CMOS	< -8	13.7	0.002–1.6	1.9	$0^{\ddagger}$	$-9^{\ddagger}$	35
[21]	0.35 μm SiGe BiCMOS	< -10	18.8	4.9–6	3.9	$-3.5^{\diamond}$	$-13.9^{\diamond}$	26.4
[5]	0.15 μm p-HEMT	< -7	16	23–30	1.6	N/A	N/A	42
[6]	0.2 μm GaAs FET	< -6	14	12–24	N/A	N/A	3–6$^{\triangleleft}$	N/A
[7]	0.15 μm m-HEMT	< -10	10	7–21.7	4	26	N/A	100

* at 6 GHz † in the 1–4 GHz range ‡ at 0.9 GHz $^{\diamond}$ at 5.5 GHz $^{\triangleleft}$ in the 12–24 GHz range

better performance. In a system like the UWB, the average NF is perhaps a better figure of merit than the spot NF. The average NF is 5.2 dB (STD) and 5.3 dB (TW). As discussed in depth in [13], the induced gate noise plays a fundamental role in the optimization of the noise performance of CMOS LNAs. However, the BSIM3 model[1] does not include this noise source [19]. We included a subcircuit noise model in our simulations to capture the basic impact of the induced gate noise on the design. The model, shown in Fig. 19, makes use of a resistor as a noise voltage source. The noise voltage is imposed on a capacitor, and the resulting noise current is fed to the output. The spectrum of the output current is therefore proportional to ω^2. The main limitation of the subcircuit model is that the generated noise is uncorrelated with the other noise sources present in the circuit, while induced gate noise is partially correlated to the drain current noise.

The two-tone test for third-order intermodulation distortion (IIP3) is shown in Fig. 20 for the STD LNA. The test is performed at 6 GHz. Tone spacing is 1 MHz. IIP3 is -6.7 dBm, and the input referred 1-dB compression point (ICP) is -15 dBm. In the inset, Fig. 20 shows IIP3 versus frequency for both LNAs. In the 4–8-GHz range, IIP3 is higher than -8.2 dBm (STD) and -10.8 dBm (TW).

Measured second-order intermodulation distortion (IIP2) is reported for both LNAs in Fig. 21 versus frequency. In the 4–8-GHz range, IIP2 is higher than -3 dBm (STD) and -10 dBm (TW). The design does not show particularly high values of IIP2 due to the single-ended topology.

The performance shown in Figs. 12–21 allows comparison between the STD and TW LNA designs. The use of triple-well devices accomplishes the goal of pushing the -3-dB cutoff frequency to higher frequencies. However, the achieved bandwidth improvement is smaller than expected from simulation results. Moreover, the enhancement of the frequency response of the amplifier comes at the price of a reduction of the reverse isolation and lower linearity.

Table II summarizes the performance of the presented amplifiers, with comparison to previously published LNAs. Note that distributed amplifiers generally consume much higher power than the proposed amplifier.

[1]BSIM4 includes a holistic thermal noise model that does take induced gate noise into account.

VI. CONCLUSION

We have demonstrated in this paper a low-power approach for the design of ultrawideband LNAs in the 3.1–10.6-GHz band. The design employs the use of a three-section reactive input network to match an inductively degenerated MOS transistor to a 50-Ω source. This allows us to achieve simultaneously a good antenna termination, low noise, high gain, and high linearity in a wideband fashion, while consuming only 9 mW. The presented design can exploit the CMOS technology evolution trends, both in terms of feature scaling, implying higher speed and lower noise for the active device, and in terms of higher Q passives. The effectiveness of our approach is supported by experiments carried out on LNA prototypes implemented in a 0.18-μm CMOS technology.

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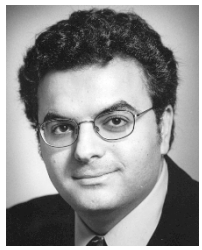
Andrea Bevilacqua (S'02) received the Laurea and Ph.D. degrees in electronics engineering from the University of Padova, Padova, Italy, in 2000 and 2004, respectively.

From 1999 to 2000, he was an intern with Infineon Technologies, Munich, Germany. From 2002 to 2003, he was a Visiting Scholar with the University of California, Berkeley. His current research interests include the design of RF/microwave integrated circuits and the analysis of wireless communication systems.



Ali M. Niknejad (S'93–M'00) received the B.S.E.E. degree from the University of California, Los Angeles, in 1994, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1997 and 2000, respectively.

From 2000 to 2002, he was with Silicon Laboratories, Austin, TX, where he was involved with the design and research of CMOS RF integrated circuits and devices for wireless communication applications. Presently, he is an Assistant Professor with the Electrical Engineering and Computer Science Department, University of California, Berkeley. He is an active member at the Berkeley Wireless Research Center (BWRC) and he is the Codirector of the BSIM Research Group. His current research interests lie within the area of analog integrated circuits, particularly as applied to wireless and broadband communication circuits. His interests also include device modeling and numerical techniques in electromagnetics.

Dr. Niknejad is currently serving as an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.