Partial Element Equivalent Circuit (PEEC)

E8-202 Class 12

Dipanjan Gope

Grading Scheme

Time Frame	Assignment	Grading
Sep 6	HW 1	15
Sep 24	HW2	
Oct 8	HW 3	
Oct 11	Midterm 1	15
Nov 5	HW 4	5
Nov 20	Midterm 2	15
Dec 5	Final Exam	30
Dec 10	Final Project	20

Module 2: Method of Moments

- 2D vs 2.5D vs. 3D Formulations
- Electrostatic Formulation: Capacitance matrix extraction
- Magnetostatic Formulation: Inductance matrix extraction
- Electric Field Integral Equation (EFIE): S-parameter extraction
- Partial Element Equivalent Circuit (PEEC) Method
- Magnetic Field Integral Equation (MFIE) and Combined Field Integral Equation (CFIE)
- PMCHWT Formulation: Dielectric modeling
- Parallelization techniques

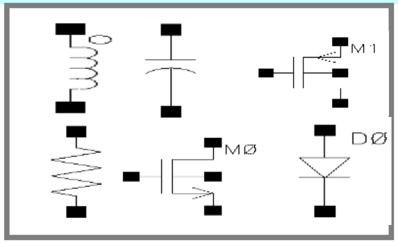
References

- A. E. Ruehli, “Equivalent circuit models for three-dimensional multiconductor systems” *IEEE Trans. Microwave Theory and Techniques*, vol. MTT22 (3), pp. 216-221, March 1974.

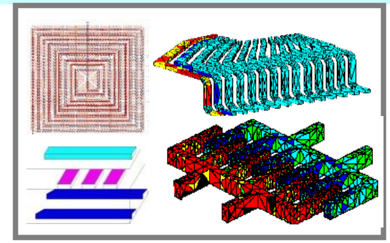
What does PEEC do?

Elements

Lumped Circuit Elements
e.g. R; L; C; V; I



Distributed Circuit Elements
e.g. Transmission Line



Definition

$t_r >> t_d$

$t_r \sim t_d$

Equations

KVL; KCL

Maxwell's Equations

Solution

SPICE

PEEC

Port Model + SPICE

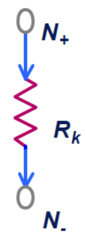
SPICE Review

- Sparse Tableau Analysis (STA)
  - IBM ASTAP simulator

- Modified Nodal Analysis (MNA)
  - SPICE simulators

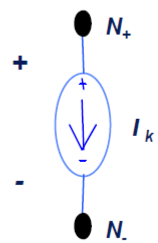
Stamps Revisited

Resistor



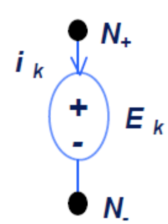
$$\begin{array}{c|ccc} & N_+ & \cdots & N_- \\ \hline N_+ & 1/R_k & & -1/R_k \\ \vdots & \vdots & & \vdots \\ N_- & -1/R_k & & 1/R_k \end{array}$$

Current Source



$$\begin{array}{c} N_+ \\ \\ N_- \end{array} \begin{bmatrix} & \\ \vdots & \vdots \\ & \end{bmatrix} = \begin{bmatrix} -I_k \\ +I_k \end{bmatrix}$$

Voltage Source

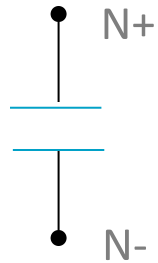


	N_+	N-	i_k	RHS
N_+	0	0	1	0
N-	0	0	-1	0
branch k	1	-1	0	E_k

Some excerpts from UW class notes by Prof. Richard Shi and Guoyong Shi

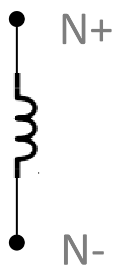
Stamps Revisited

Capacitor



	N+	N-	RHS
N+	C/h	-C/h	(C/h)V(t-h)
N-	-C/h	C/h	-(C/h)V(t-h)

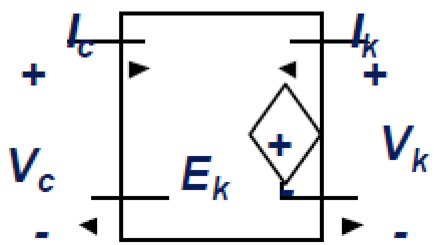
Inductor



	N+	N-	I-branch	RHS
N+			1	
N-			-1	
Branch	1	-1	-L/h	-(L/h)I(t-h)

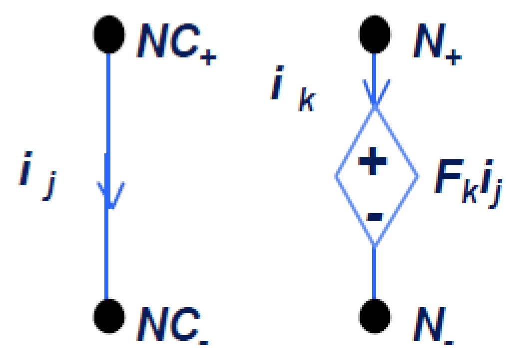
Stamps Revisited

VCVS



	N+	N-	NC+	NC-	ik
N+					1
N-					-1
NC+					
NC-					
ij	1	-1	E	-E	

CCCS



	N_+	N-	NC_+	NC-	i_k	i_j
N_+					1	
N-					-1	
NC_+						1
NC-						-1
branch k	1	-1				$-F_K$
branch j			1	-1		

Some excerpts from UW class notes by Prof. Richard Shi and Guoyong Shi

PEEC: Equation

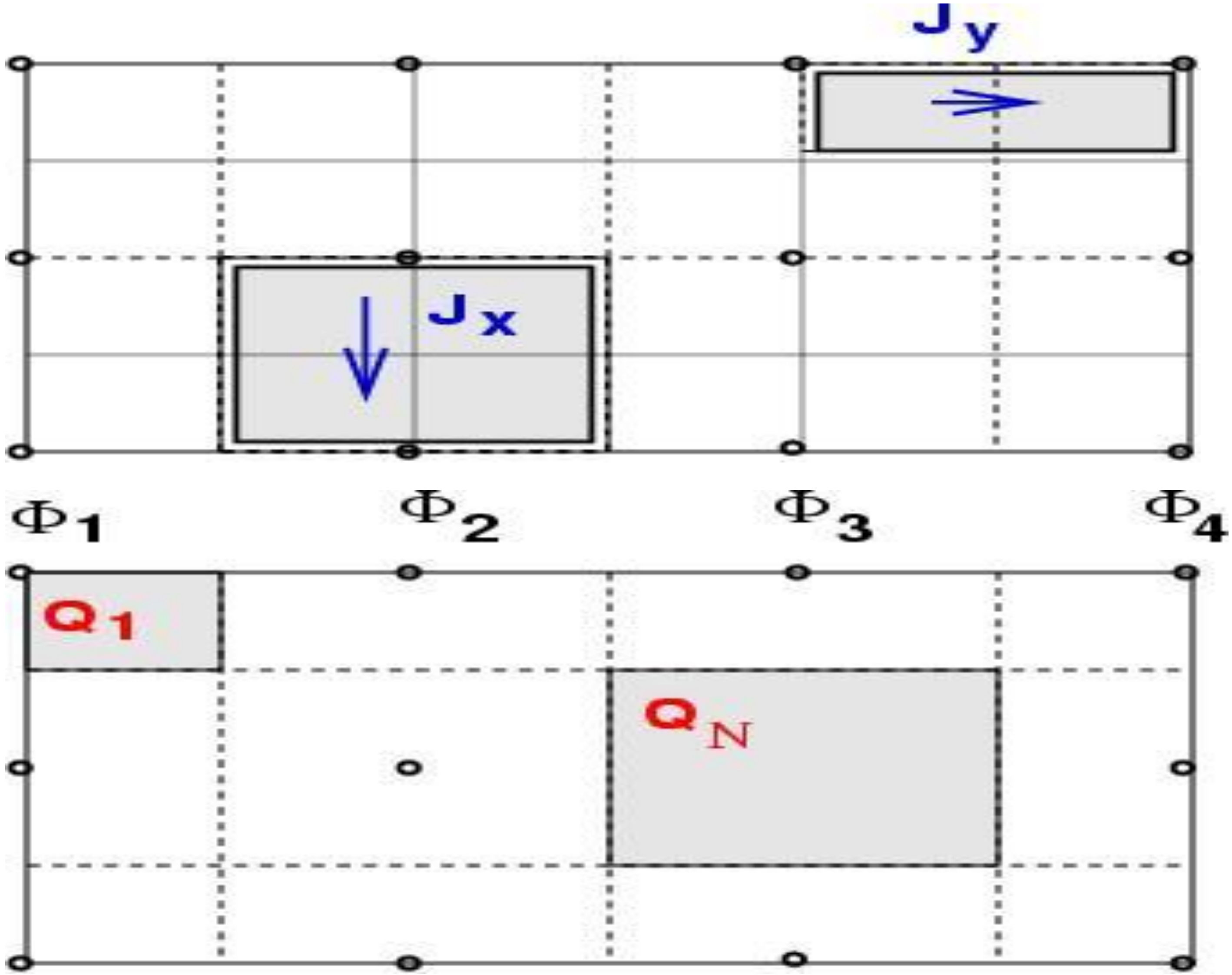
$$\bar{E}^{i}(\bar{r},\omega) = \frac{\bar{J}(\bar{r})}{\sigma} + j\omega\mu\int_{v'} G(\bar{r},\bar{r}')\bar{J}(\bar{r})dv' + \frac{\nabla}{j\omega}\int_{v'} G(\bar{r},\bar{r}')q(\bar{r})dv'$$

Circuit Model Element Identification

- KVL: Voltage = R I + sLp I + Q/sC
- RHS Term 1: Resistance
- RHS Term 2: Partial Inductance
- RHS Term 3: Coefficients of Partial Potential

Basis Function

Current

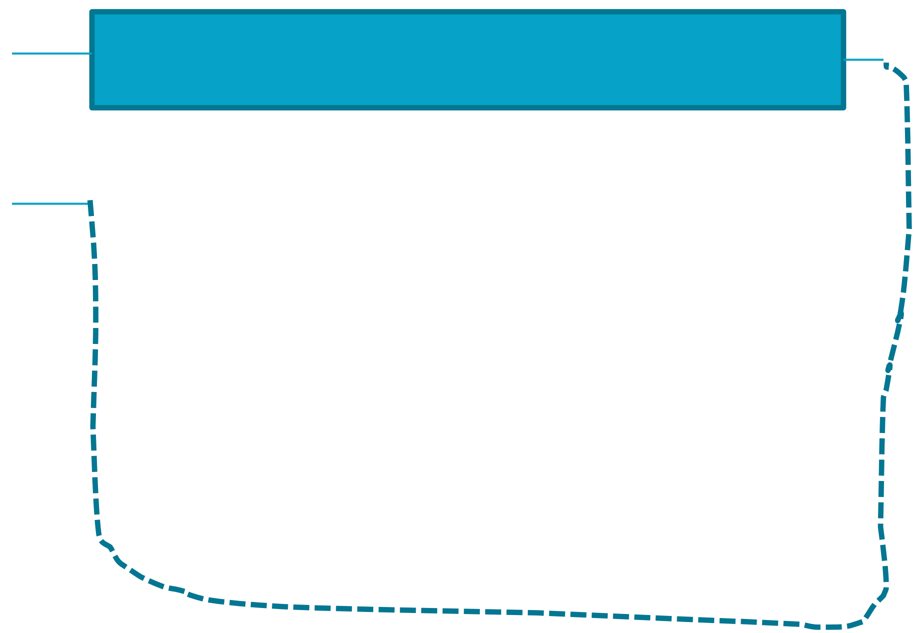


Charge

Partial vs Loop Inductance

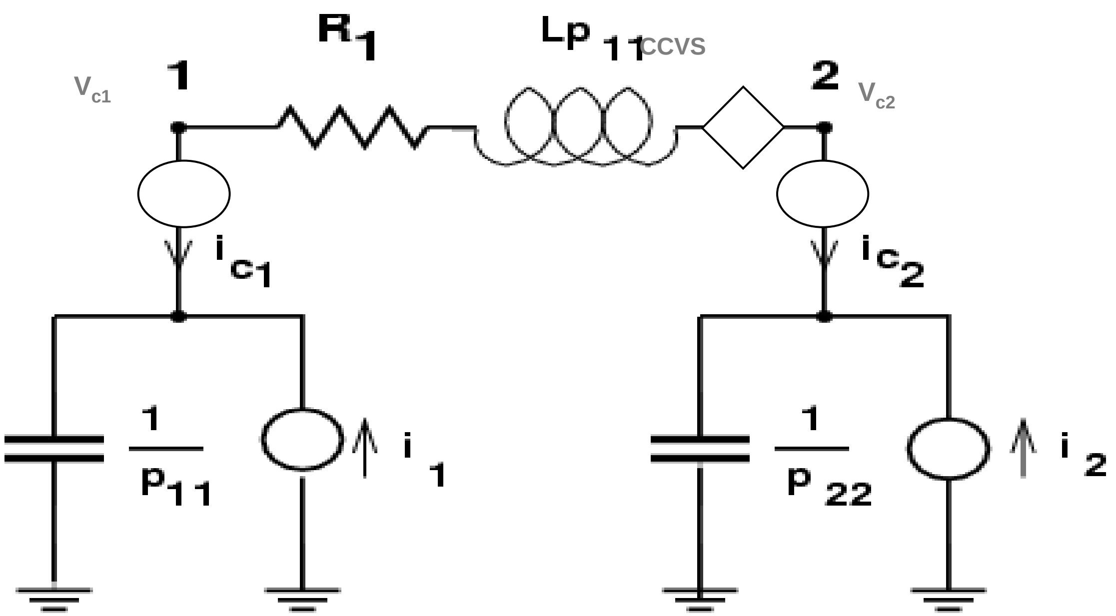
Loop

Partial



$$L = L_{11} + L_{22} - 2L_{12}$$

Unit Cell

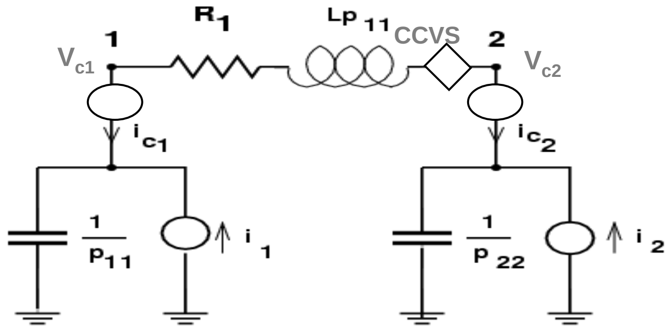


$$\bar{E}^{i}(\bar{r},\omega)=\frac{\bar{J}(\bar{r})}{\sigma}+j\omega\mu\int_{v'}G(\bar{r},\bar{r}')\bar{J}(\bar{r})dv'+\frac{\nabla}{j\omega}\int_{v'}G(\bar{r},\bar{r}')q(\bar{r})dv'$$

Testing Function

$$\frac{1}{a_{\alpha}}\int_{v_{\alpha}}f(r)dv=\frac{1}{a_{\alpha}}\int_{a_{\alpha}}\int_{l_{\alpha}}f(r)da\,dl$$

Resistance Term

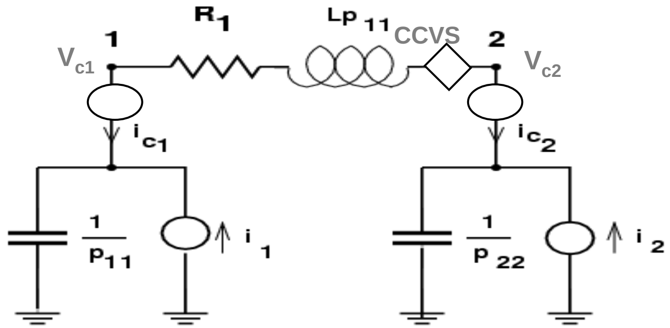


$$\frac{1}{a_\alpha}\int_{v_\alpha}\frac{J}{\sigma}dv = \frac{1}{a_\alpha}\int_{a_\alpha}\int_{l_\alpha}\frac{J}{\sigma}da\,dl$$

$$\frac{1}{a_\alpha}\int_{v_\alpha}\frac{J}{\sigma}dv = \frac{1}{a_\alpha}\int_{a_\alpha}\int_{l_\alpha}\frac{I}{a_\alpha\sigma}da\,dl$$

$$\frac{1}{a_\alpha}\int_{v_\alpha}\frac{J}{\sigma}dv = \frac{I}{\sigma}\frac{l}{a_\alpha}$$

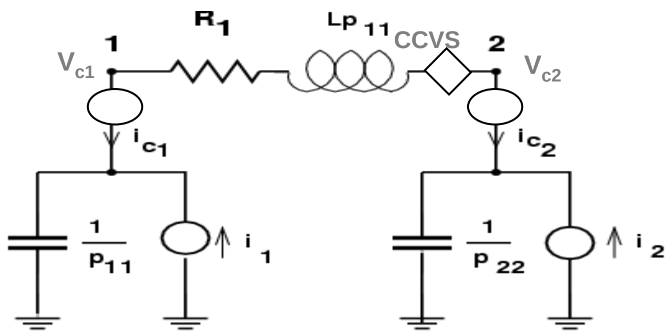
Inductance Term



$$\frac{1}{a_\alpha}\int_{a_\alpha} j\omega \int_{a_{\alpha'}} GJdvdv' = j\omega \frac{1}{a_\alpha a_{\alpha'}} \int_v \int_{v'} Gdvdv'$$

$$L_{p_{vv'}} = \frac{1}{a_\alpha a_{\alpha'}} \int_v \int_{v'} Gdvdv'$$

Capacitor Terms



$$\phi_1 = p_{11}Q_1 + p_{12}Q_2$$

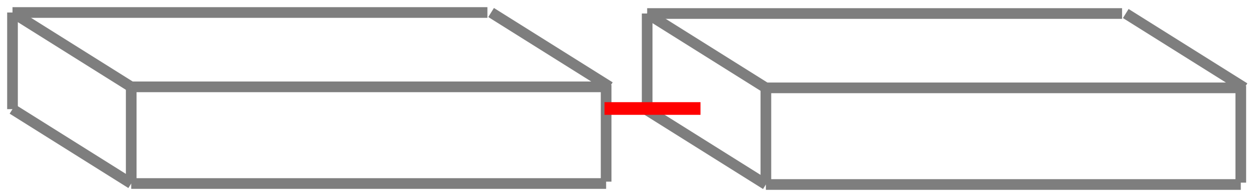
$$\frac{1}{p_{11}}\phi_1 = Q_1 + \frac{p_{12}}{p_{11}}Q_2$$

$$\frac{1}{p_{11}}\frac{d\phi_1}{dt} = \frac{dQ_1}{dt} + \frac{p_{12}}{p_{11}}\frac{dQ_2}{dt}$$

$$\frac{1}{p_{11}}\frac{d\phi_1}{dt} = i_{c1} + \frac{p_{12}}{p_{11}}i_{c2}$$

PEEC Stick Example

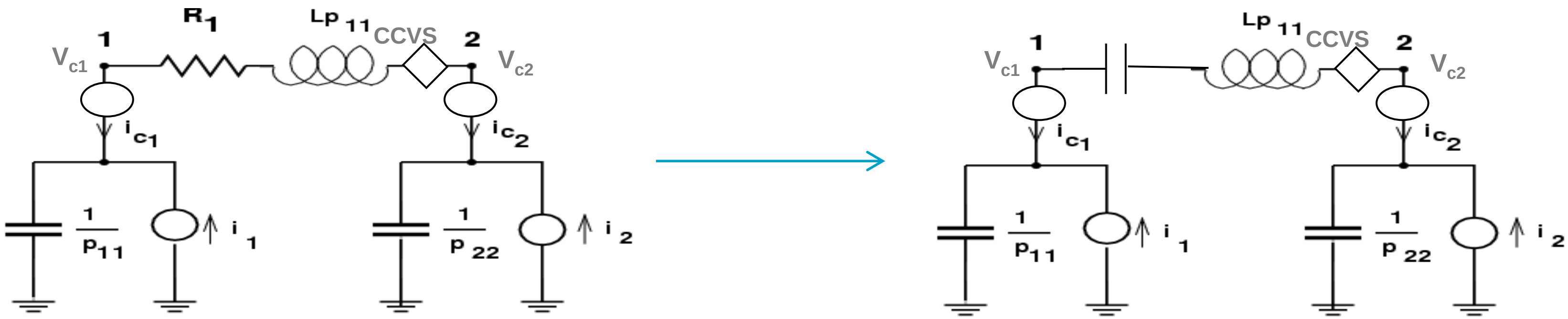
Geometry



Conductor

R1	N1	N2		1.202mOhms		
L1	N2	N3		5.887nH		
C1	N1	0		1.702pF		
K12	L1	L2		1.282nH	0.054ns	
F12	N4	0	V1	0.124		0.032ns

Basic Dielectric Modeling



$$E^{i}(r,\omega) = \frac{J}{j\omega(\varepsilon - 1)\varepsilon_0} + j\omega\int_{v'} G(r,r')J(r')dv' + \frac{\nabla}{j\omega}\int_{v} G(r,r')q(r')dv'$$

$$C = (\varepsilon - 1)\varepsilon_0 \frac{A}{l}$$

PEEC Flow

1. Integral Equation Solution to Maxwell's Equations
2. Special Meshing for PEEC Cells
3. Transformation to PEEC Circuit Elements
4. SPICE Like Circuit Description (inputs: Transformation to PEEC Circuit Elements, plus:)
   - SPICE Circuit Elements
   - Other SPICE Type Models
5. MNA Delay Diff. Eq. (DDE) Circuit Solver
6. Voltages, Currents, Electric and Magnetic Fields

PEEC History

- Orthogonal, No-retardation
- …
- Orthogonal, with-retardation
- …
- Orthogonal, with-dielectric and retardation
- Non-orthogonal, with dielectric, retardation
- ….

PEEC: Advantages

- Volumetric formulation ideal for on-chip cases
  - No thickness discretization necessary
- DC to daylight solution
  - Charge and current decoupled at DC
- “Stamps” provide interface between techniques
- Multi-purpose solver (.tran / .ac / .cap / .ind)

PEEC: Drawbacks

Dense Matrix: Expensive LU (Gaussian Elimination)
- **Can we use EM properties to expedite solution?**

Volume formulation unsuitable for “thick” structures
- **Can we get similar stamps for surface-based/hybrid form?**

Addressed in later research