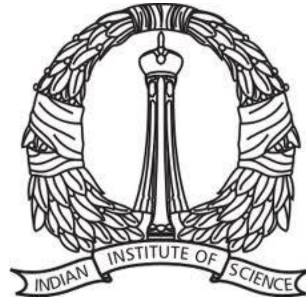
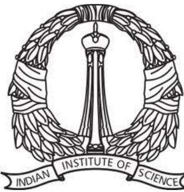


E8-262: CAD for High-Speed Chip-Package-Systems

Module 1: Electrical Challenges in High-Speed CPS

- Types of packages and PCBs
- Packaging Trends
- Review of Electromagnetic and Circuit basics
- Signal Integrity
- Power Integrity
- Electromagnetic Interference and Electromagnetic Compatibility
- Review of SPICE basics
- Lumped models, distributed RLGC, S/Y/Z parameters



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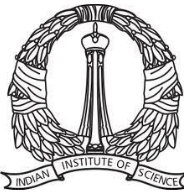
Function of Packages

- Power Distribution
- Signal Distribution
- Heat Dissipation
- Mechanical stability or package protection



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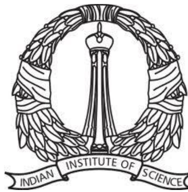
Desired Package Properties

- Electrical performance
  - High speed (short delay)
  - High bandwidth
  - High Pin Count
  - Power distribution with low R
  - Power distribution with low L
- Thermal performance
- Mechanical performance



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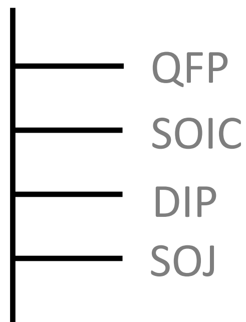
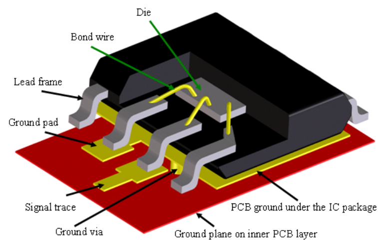
Types of Packages

Based on connection to Printed Circuit Board

Lead Frame Packages



- Cheap
- Low Pin Count
- Wire bonding



http://www.iue.tuwien.ac.at/phd/poschalko/img410.png

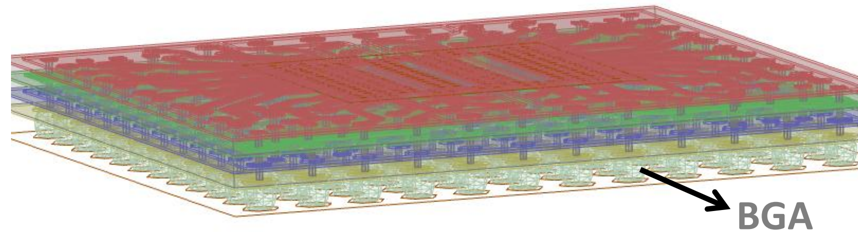
Grid Array

Ball Grid Array

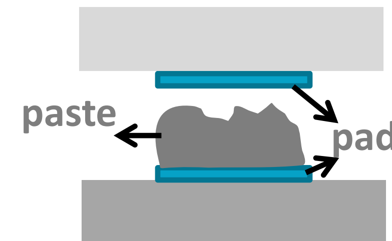
- Smaller
- Routable substrate
- High pin count

Land Grid Array

- Pad and paste
- Routable substrate
- Cheaper than BGA
- Better electrical perf.



Visualization: Courtesy Nimbic



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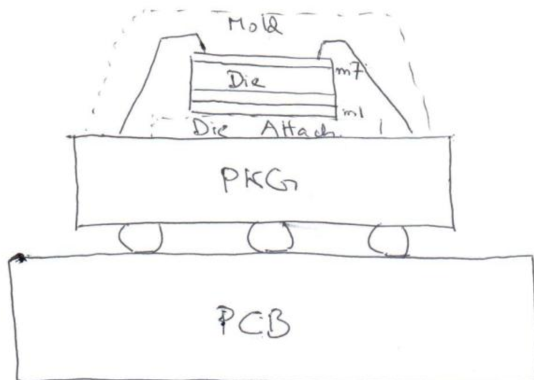
Types of Packages

Based on connection to Die

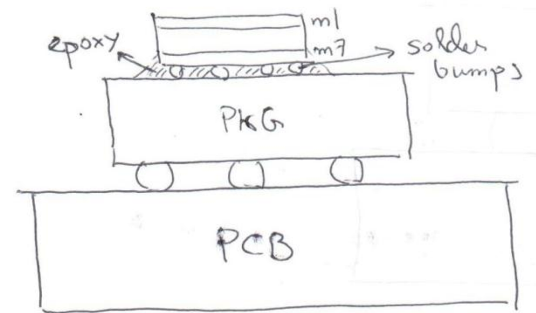
Wire Bond

- Gold wire (also Al, Cu)
- Inexpensive
- Reliable

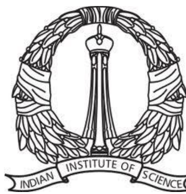


Flip Chip

- Solder bumps, under-fill epoxy
- Controlled Collapsible Chip Connection
- Lower inductance
- Smaller package size



Tape Automatic Bond



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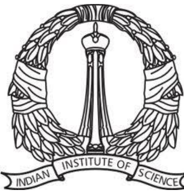
Chip Scale Package (CSP)

- Chip size ~ package size (typically 120%)
  - Smaller package
  - Lighter package
  - Tolerant to die-size change



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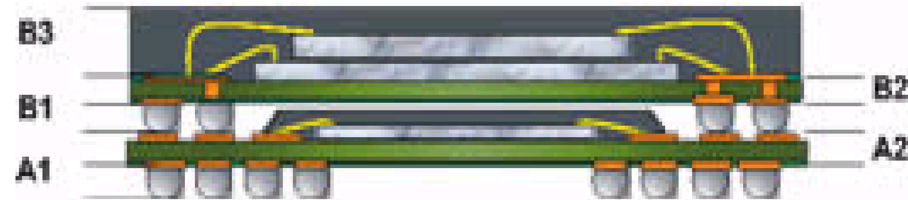
Package-on-package (PoP)

- Package on package
  - Memory-Memory
  - Logic-Memory
  - Minimized track-length, better electrical performance



www.amkor.com

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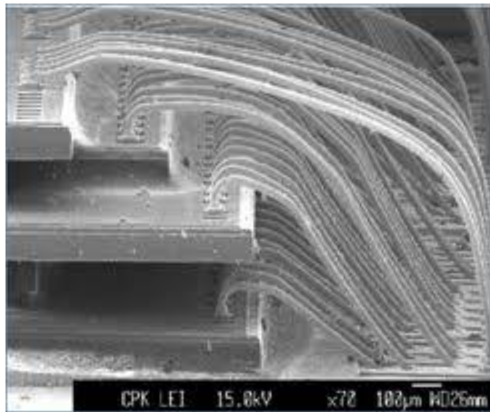
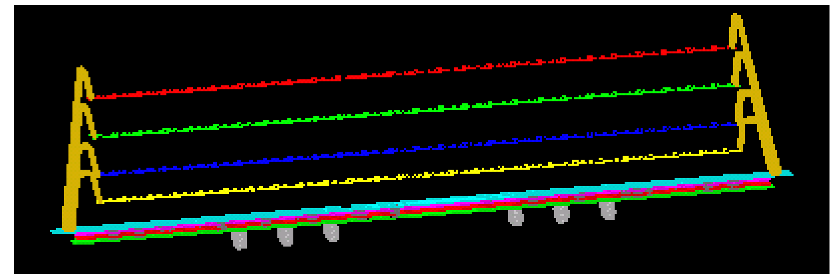
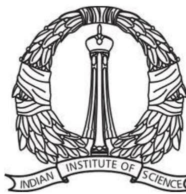
Stacked Die

- 2 or more dies stacked on top
  - Wire bond connections
  - Smaller, thinner, lighter
  - Reduced costs
  - Memory intensive applications



http://www.palomartechnologies.com





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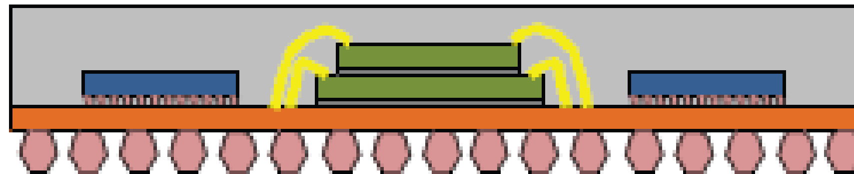
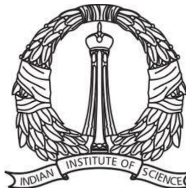
System-in-Package (SiP)

- Integration of multiple ICs, discrete components into 1 package
  - Mixed technology support (CMOS, SiGe)
  - Inexpensive integration
  - Smaller form factor
  - Popular for hand-helds



[1] V. Jandhyala, D. Gope, S. Chakraborty, F. Ling, X. Wang, D. Williams and J. Pingenot, "3D Chip-Package-Board Modeling",*Printed Circuit Design and Fab.,* pp. 24-28, Nov 2008.



System-on-Chip

- Integration of multiple functionalities, discrete components into 1 chip
  - Digital
  - Analog
  - RF
  - Opto-electronics
  - Buses and interconnects
  - Discrete components
  - MEMS

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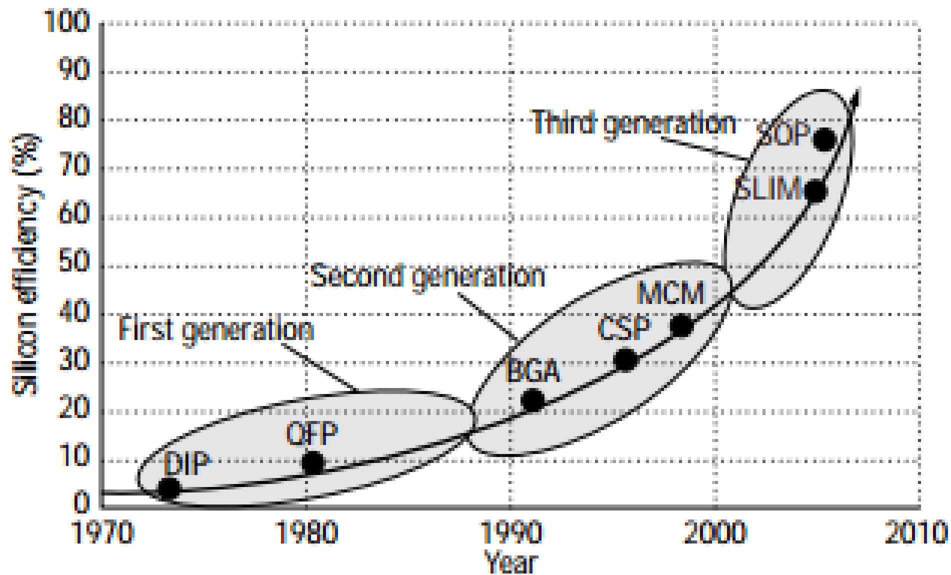
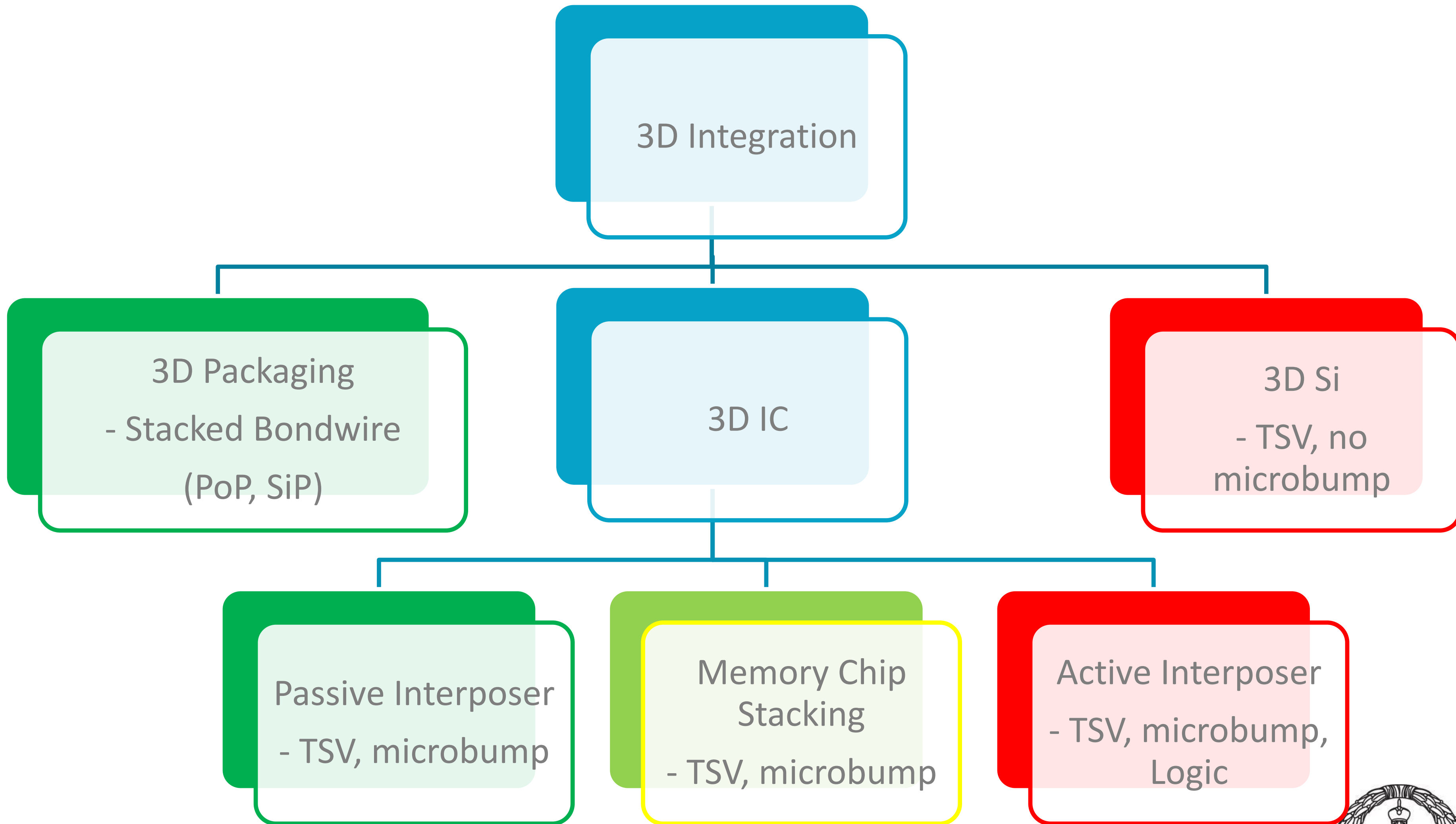
Past Trends



System on chip or system on package? – Tummala 1999

3D Integration



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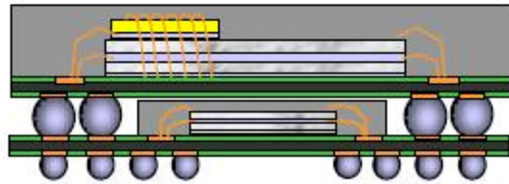
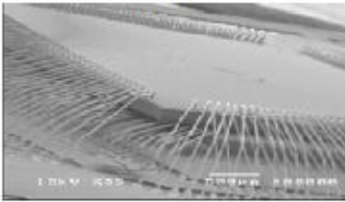
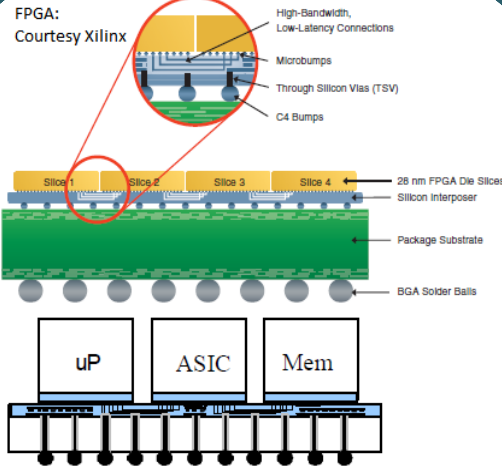
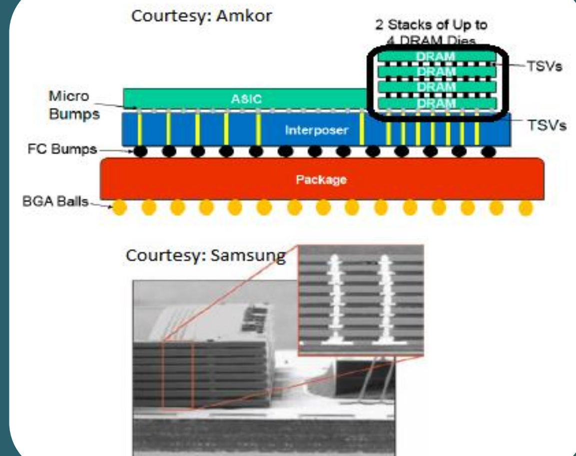
3D Integration Today



Courtesy: Amkor





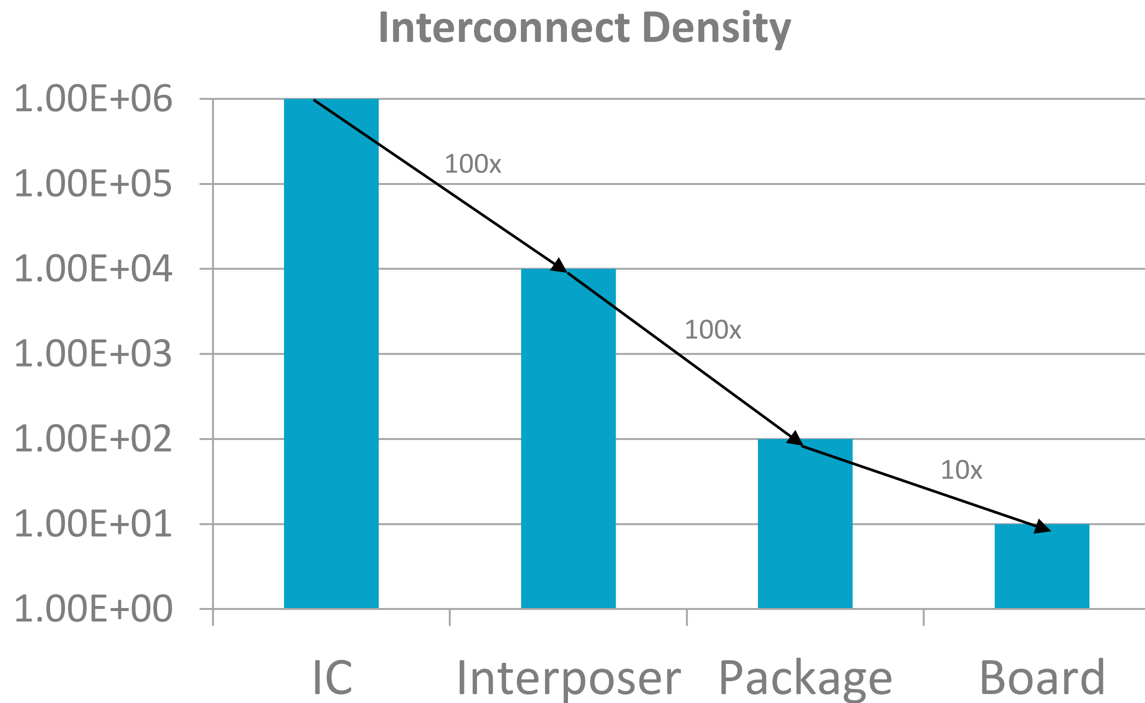


3D Packaging

Passive Interposer

Memory Chip-stacking

Interconnect Density



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