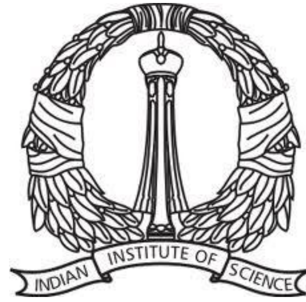

E8-262: CAD for High-Speed Chip-Package-Systems

Lecture: 2+3

Module 1: Electrical Challenges in High-Speed CPS

- Types of packages and PCBs
- Packaging Trends
- Review of Electromagnetic and Circuit basics
- Signal Integrity Introduction
- Power Integrity Introduction
- Electromagnetic Interference and Electromagnetic Compatibility Introduction
- Review of SPICE basics
- Lumped models, distributed RLGC, S/Y/Z parameters

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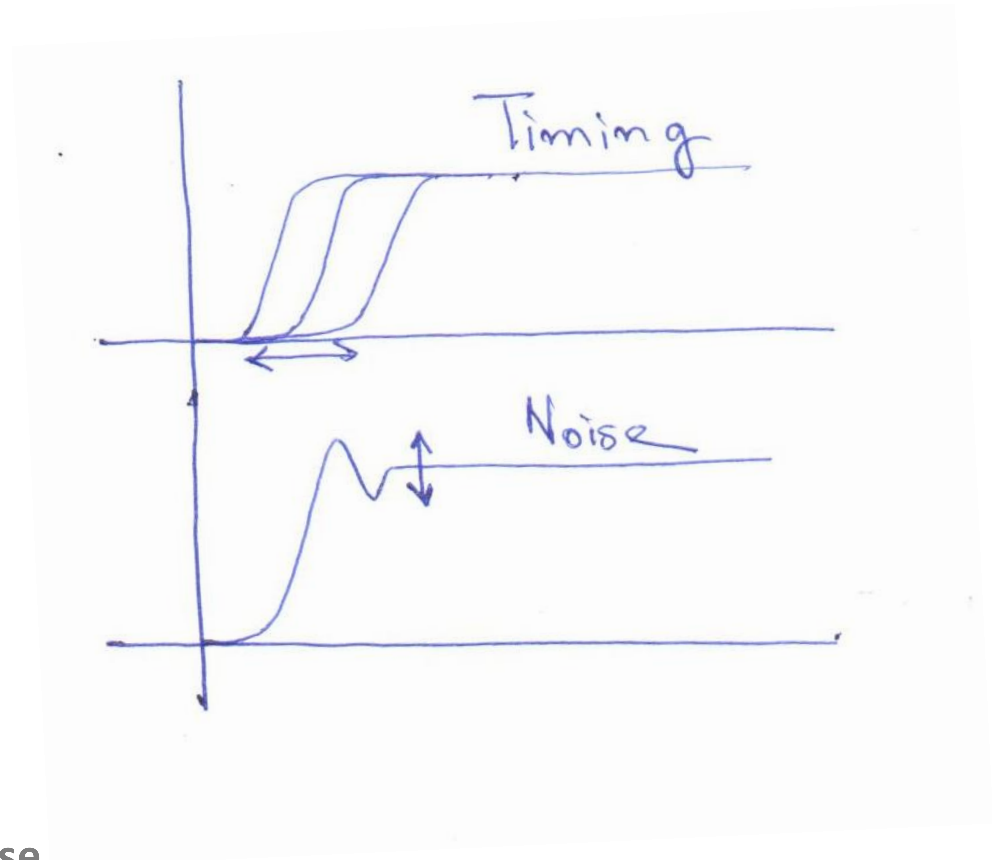
Signal Integrity: On-Chip

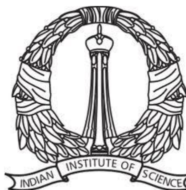
- Noise Analysis
- Timing Analysis



Sources of Noise:

1. **Interconnect or parasitic noise**
2. Propagated Noise
3. Charge-Sharing Noise
4. Power-supply noise

Harmony: static noise analysis of deep submicron digital integrated circuits; Shepard, K.L.; Narayanan, V.; Rose, R. "Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on 1999 , Page(s): 1132 - 1150



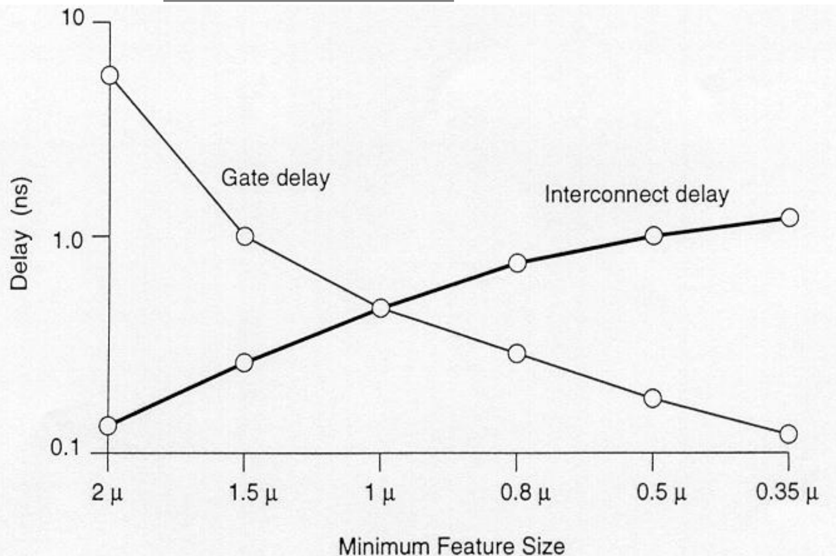
Interconnect Noise Importance: Facts

Switching Characteristics Dictate Operating Speed of Digital Systems

Capacitance in RC Delay estimation

Gate Delay

Interconnect Delay



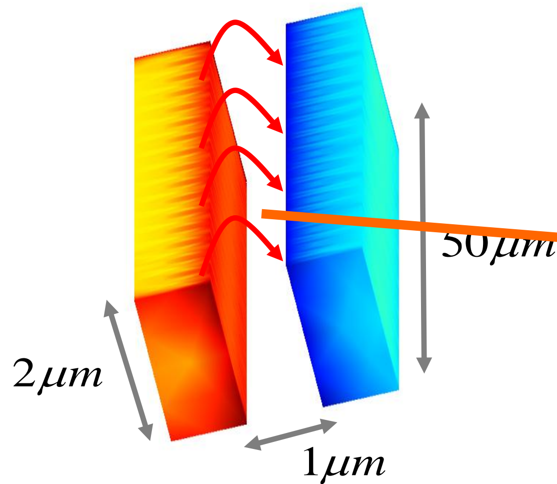
Courtesy: VLSI Systems WPI web-course

Feature Size	250nm	70nm
Gate Delay	0.075ns	0.029ns
2cm Wire Delay	2.12ns	3.53ns

Courtesy: SRC ITRS 2001

Interconnect Noise Importance: Reasons

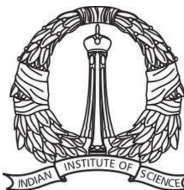
Geometry Aspect



- $|C_{12}| = 0.0069\text{pF}$
- Spacing between traces reduced
  - $|C_{12}| = 0.0103\text{pF}$
- Aspect Ratio (H/W) Increases
  - $|C_{12}| = 0.0153\text{pF}$

Size	250nm	70nm
Spacing	340nm	100nm
H/W	1.8:1	2.7:1

ITRS Data



Methodology

- Channel-Connected-Components
- RC Extraction
  - Random Walk
  - 3D solver + Pattern Matching
- Worst case vector generation
- SPICE simulation of CCC

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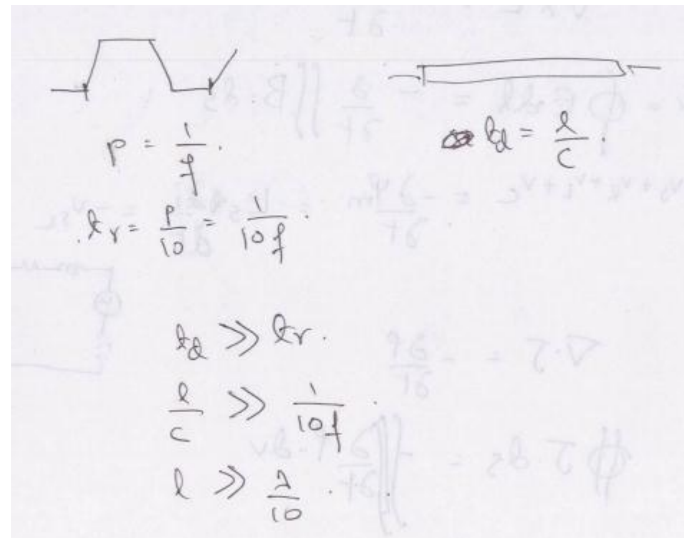
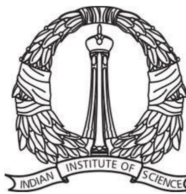
Signal Integrity: High Frequency Aspect

- What is high frequency for interconnect?

1. Delay



2. Inductive effects become significant $R + j\omega L$



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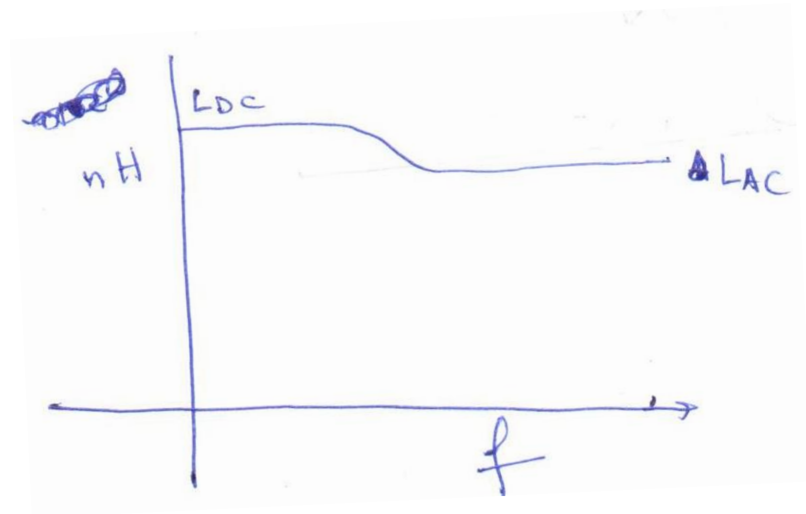
Skin Effect: R vs. L



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Interconnect Modeling for SI

- R
- RC
- RLGC: Transmission Lines – Module 2
- S-params: Full-Wave – Module 4

Channel Simulation: SPICE + S-params
Eye Diagram
TDR-TDT

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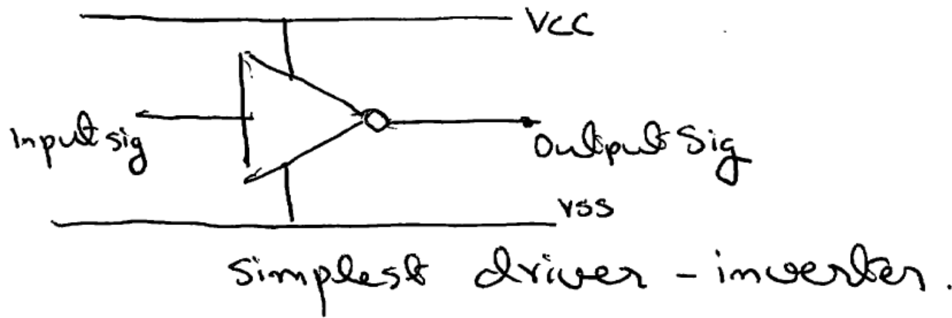
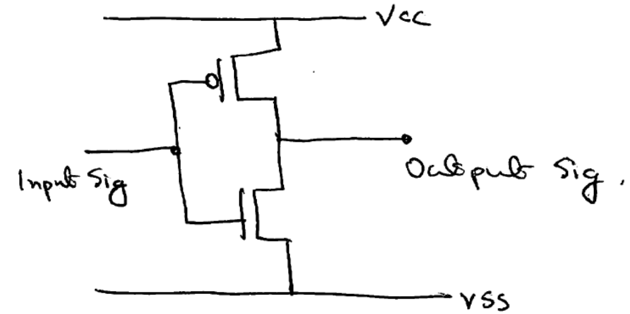
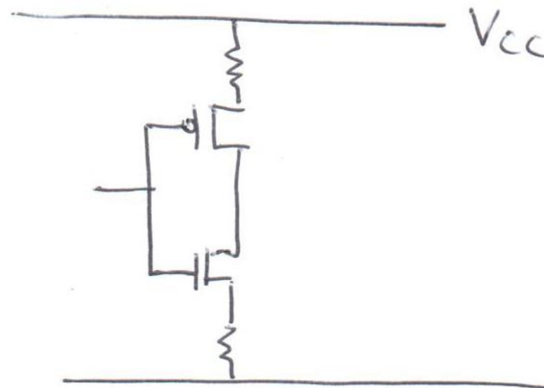
Power Integrity







DC Power Integrity

IR drop plot over PDN
Sense-line placement
Current through vias

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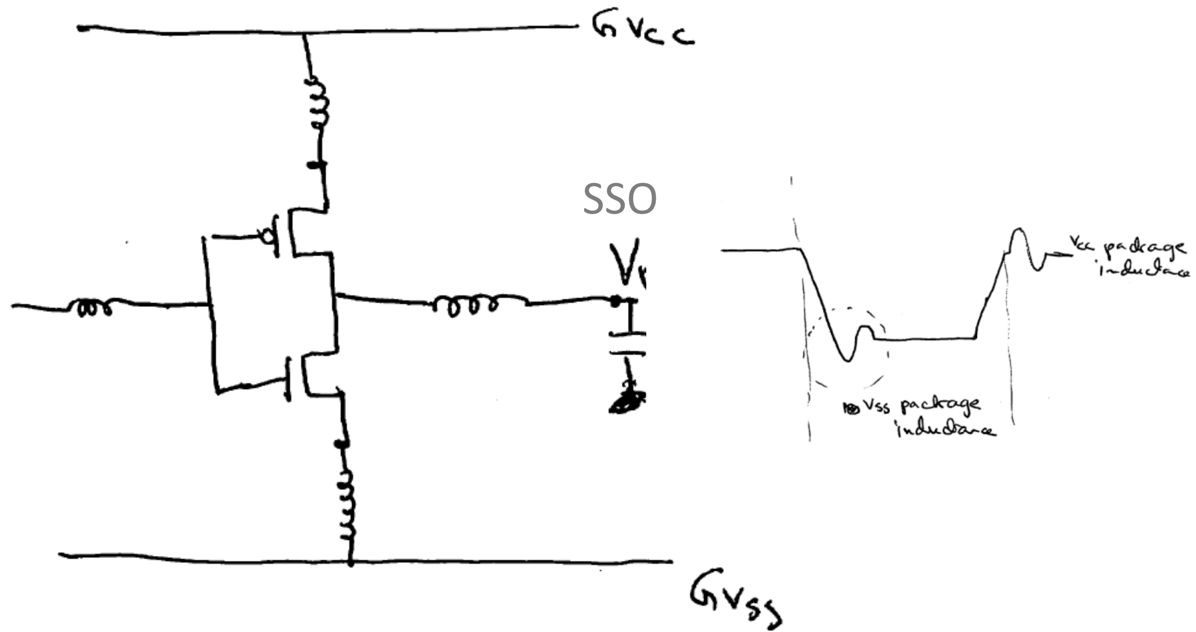
Simultaneous Switching Noise (SSN)



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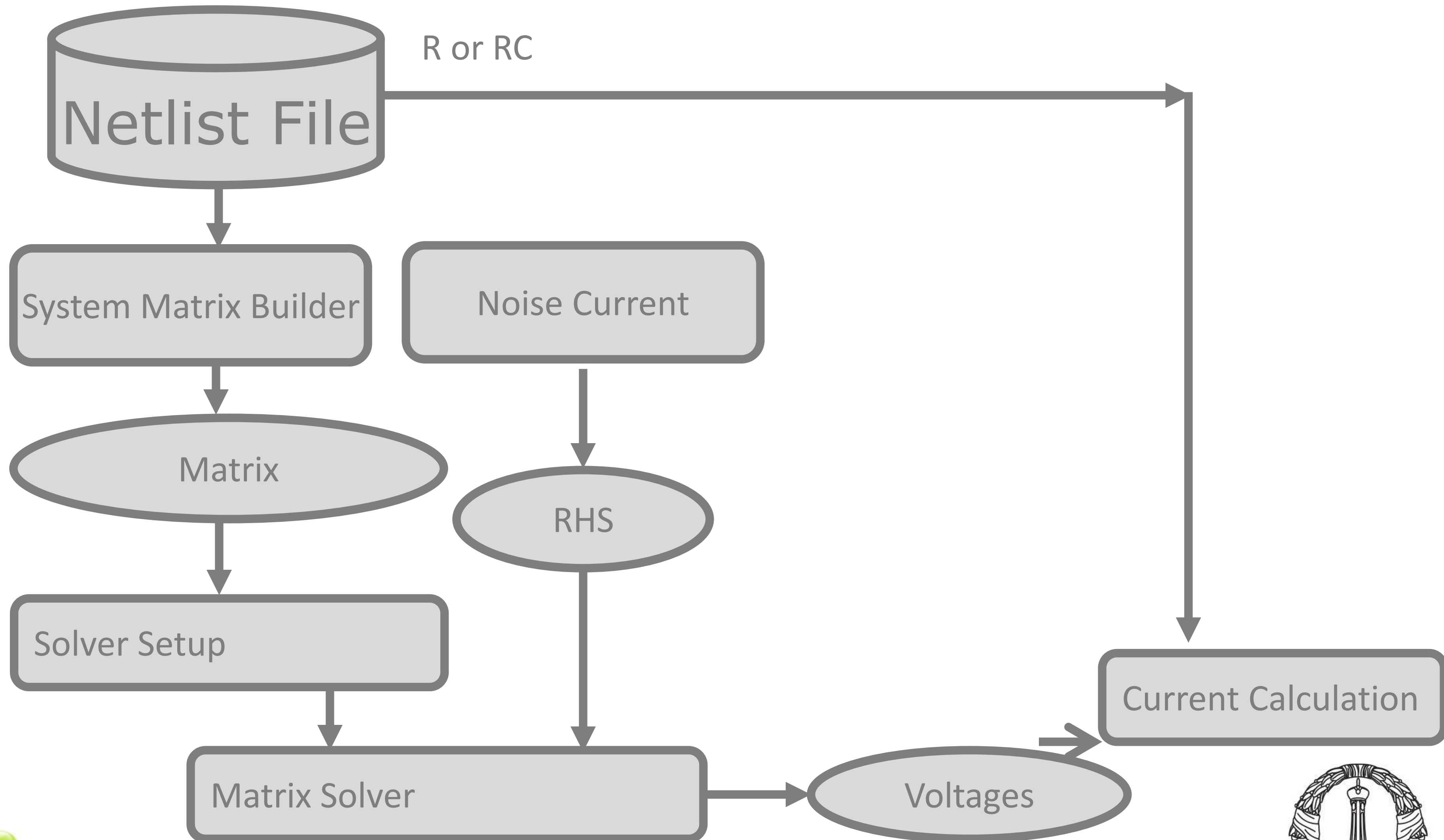
Power Integrity: On-Chip: Methodology



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Cholesky

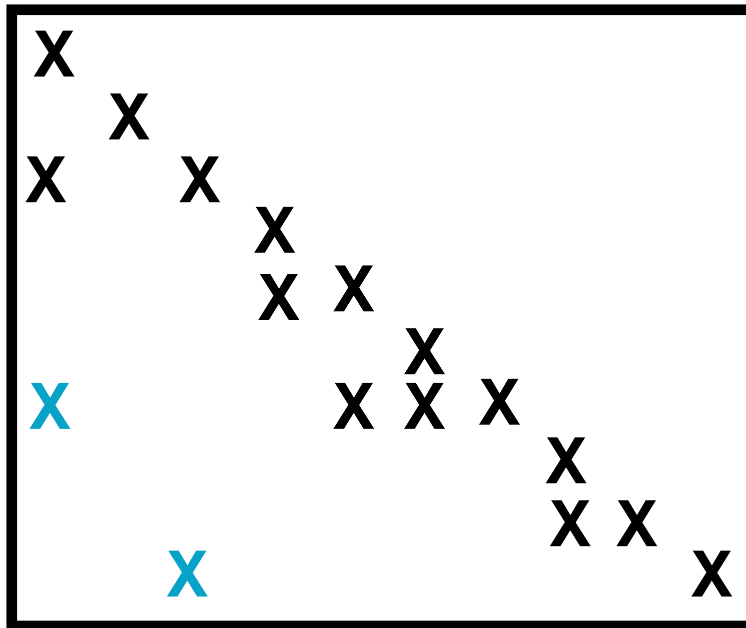
$$A(:,j) = \sum_{k=1}^{j} G(j,k)G(:,k)$$

$$G(j,j)G(:,j) = A(:,j) - \sum_{k=1}^{j-1} G(j,k)G(:,k) = v$$

```
for j=1:n
        v(j:n) = A(j:n,j);
      for k=1:j-1
        v(j:n)=v(j:n)-G(j,k)G(j:n,k);
        end
        G(j:n,j) = v(j:n)/sqrt(v(j))
end
```

DC Power Grid Solver

- R only Symmetric Positive Definite: Cholesky



Before Cholesky

After Cholesky

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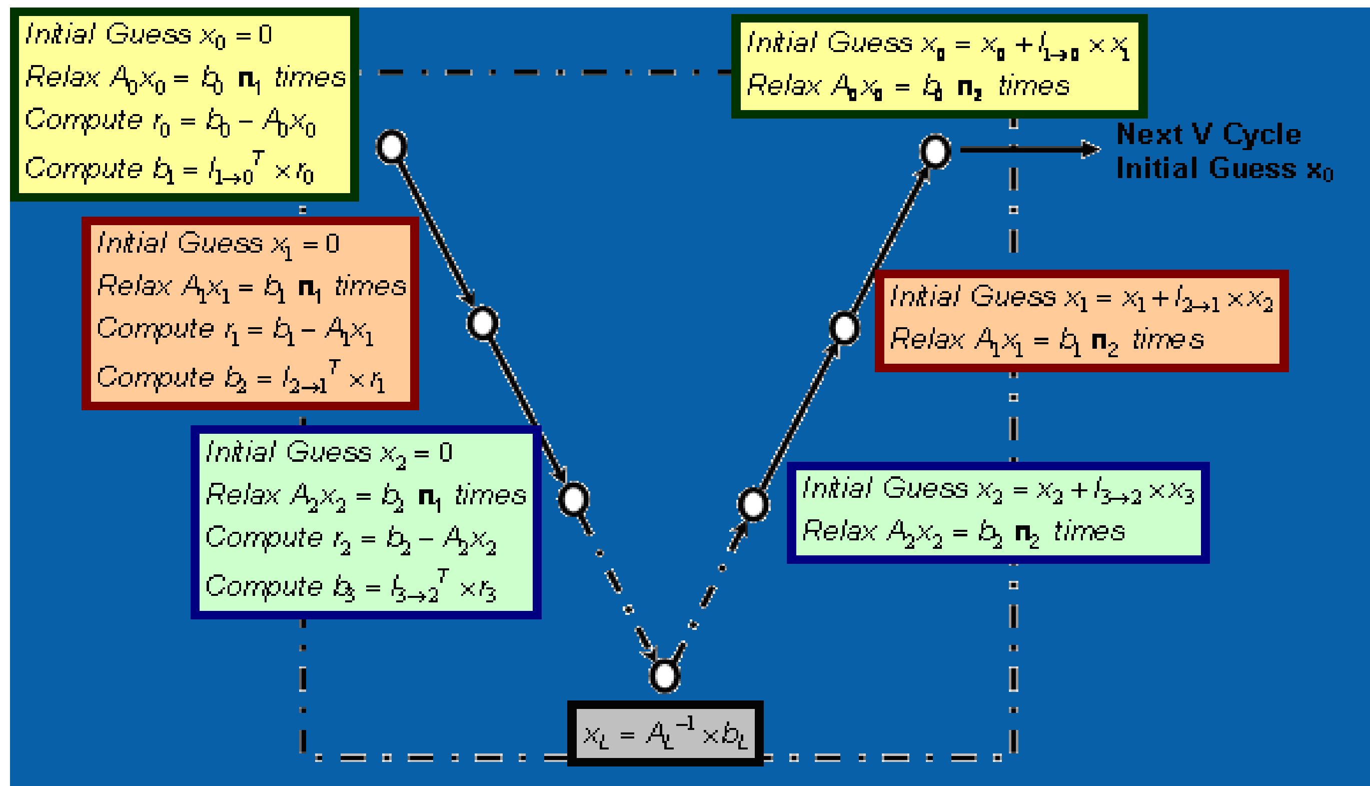
DC Power Grid Solver

- Multigrid Iterative Solvers



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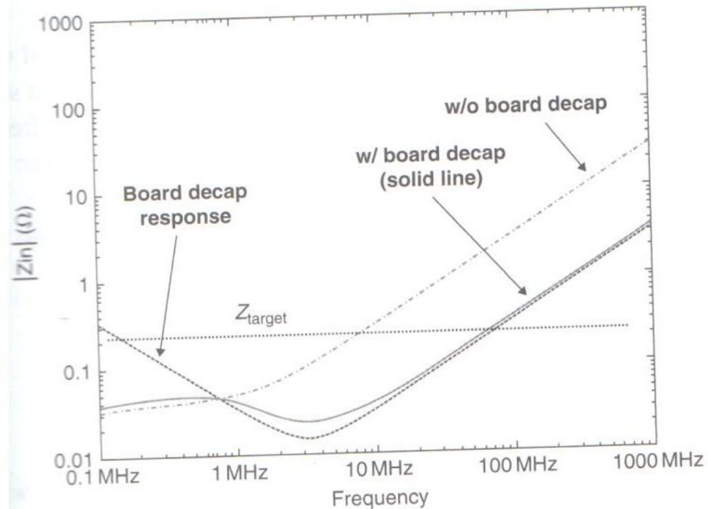
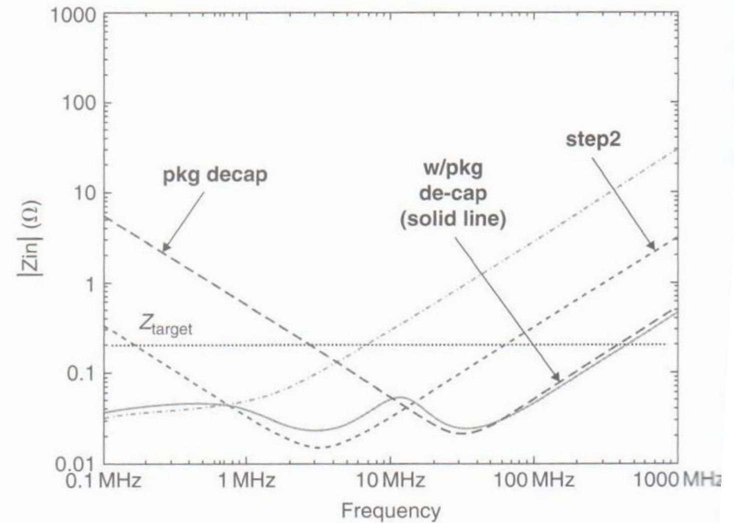
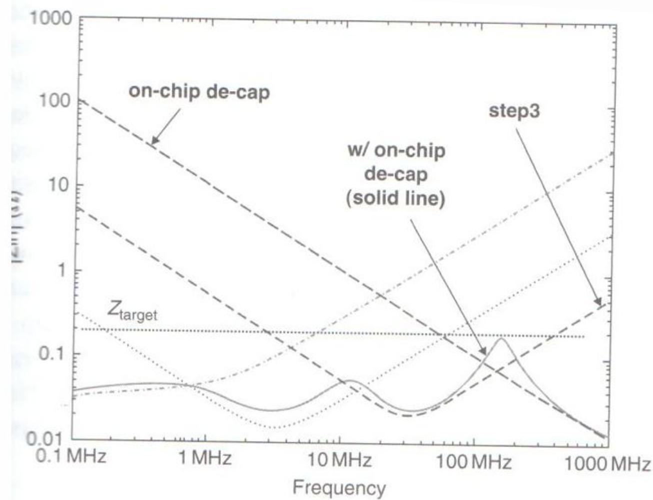
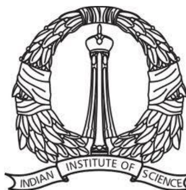
AC Power Integrity







Power Integrity Analysis and Management for Integrated Circuits,
Raj Nair and Donald Bennett, Prentice Hall Modern Semiconductor Design Series, 2010.



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Interconnect/Plane Modeling for PI

- R
- RC
- RLGC: MFDM – Module 3
- Z-params: Full-Wave – Module 4

Z Params
Ground bounce

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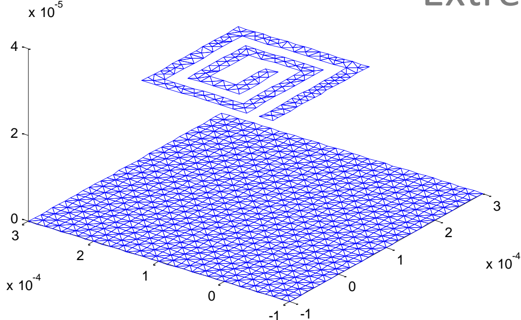
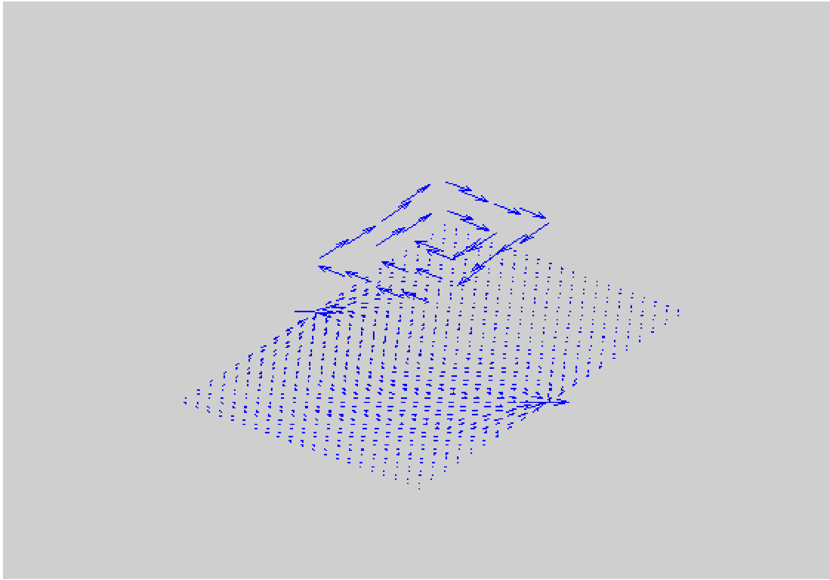
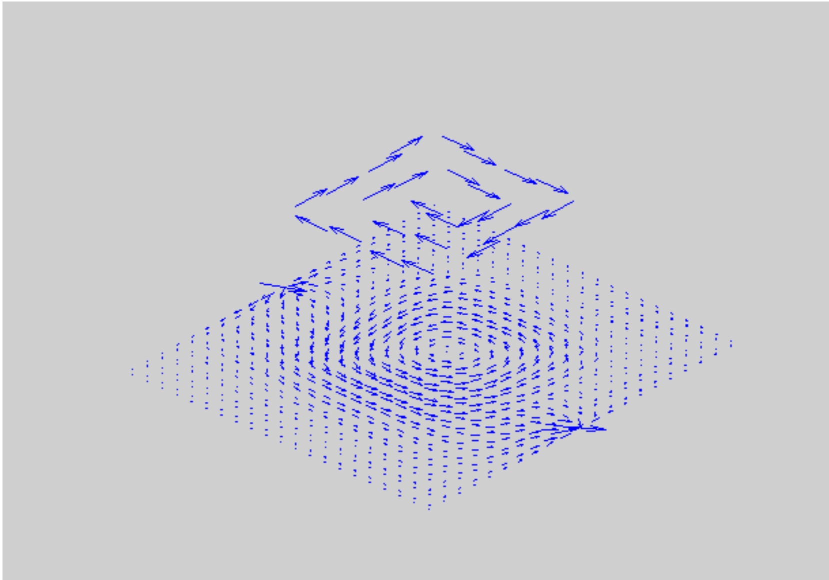
Importance of Inductance

Extreme Case: Inductor on ground plane





Low: Resistance Dominates



High: Inductance Dominates

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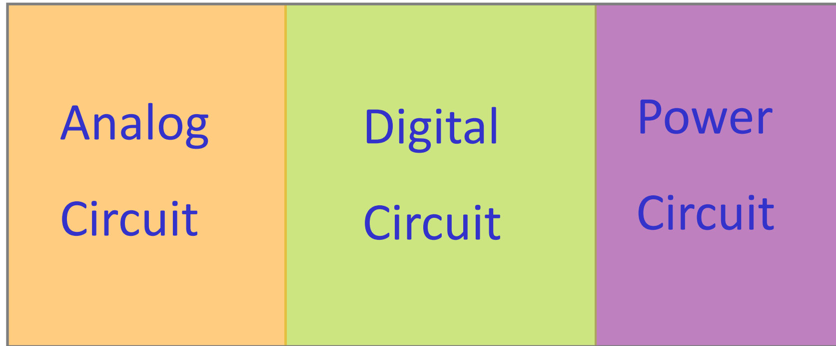
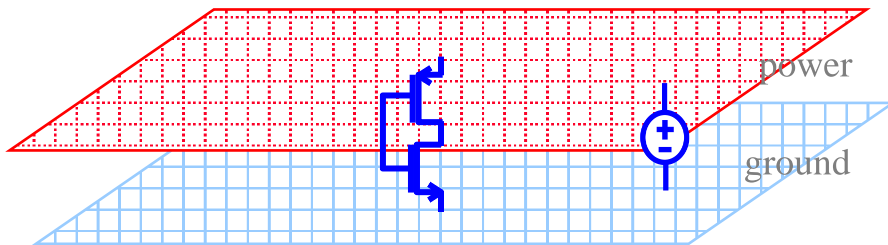
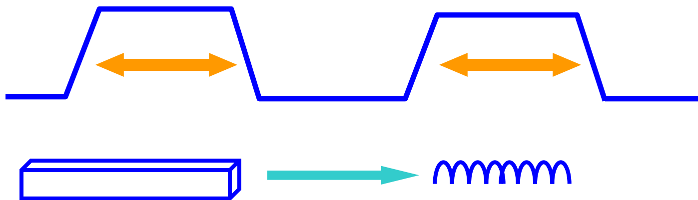
Ground Bounce

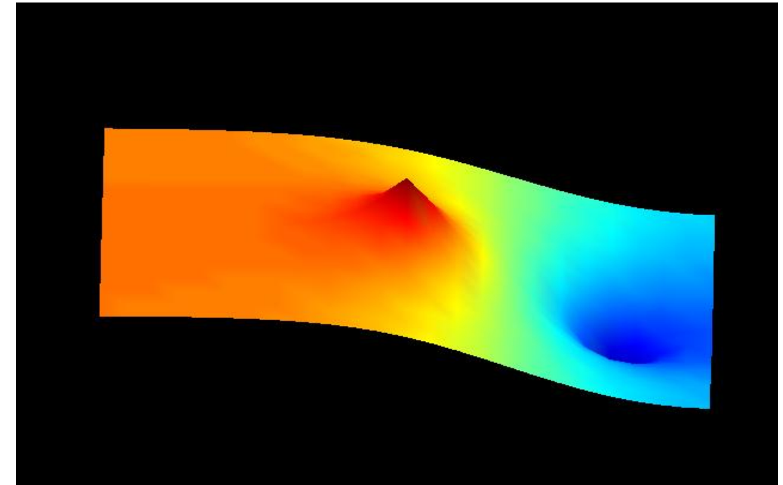


Typical Mixed Signal Board

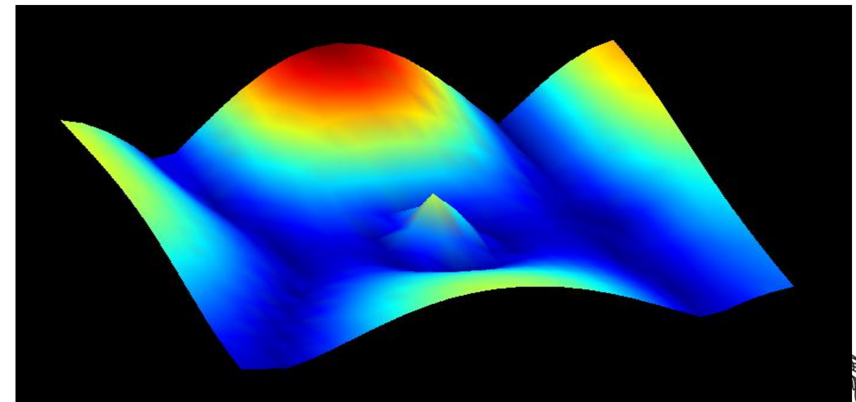


High Speed Switching noise





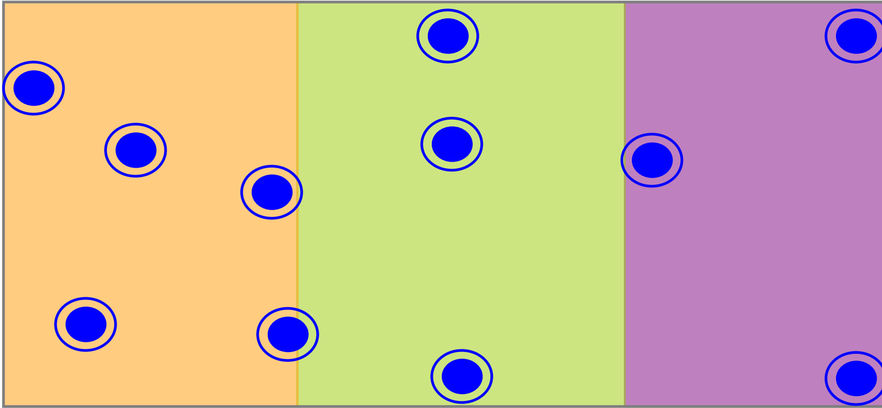
Voltage Fluctuation @ 100MHz (Max = 0.8mV)

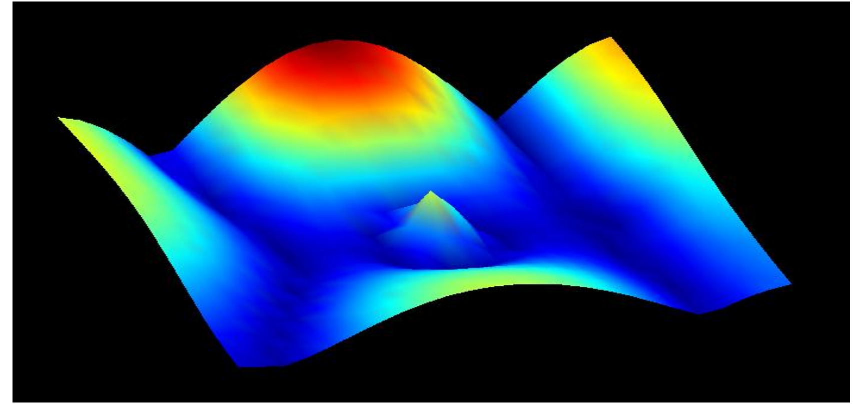


Voltage Fluctuation @ 3GHz (Max = 10mV)

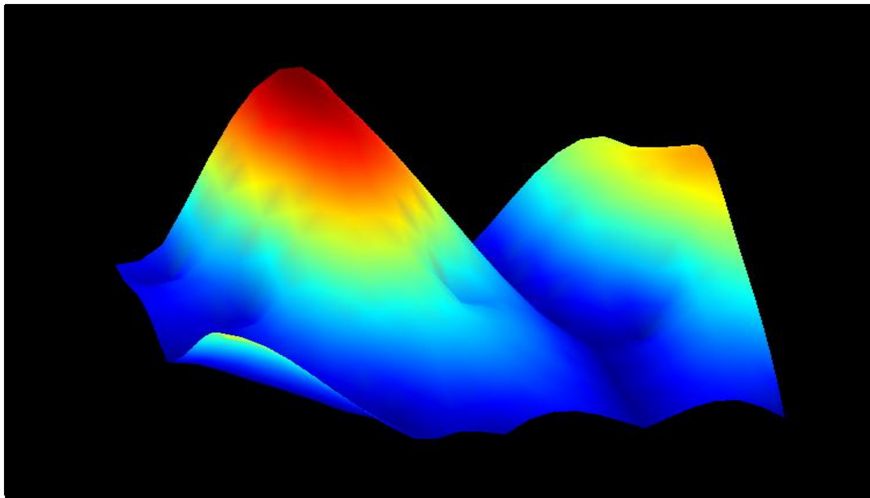
Yong Wang, Dipanjan Gope, Vikram Jandhyala and C.J. Richard Shi, "Generalized KVL-KCL Formulation for Coupled Electromagnetic-Circuit Simulation with Surface Integral Equations", *IEEE Transactions on. Microwave Theory Tech.*, vol. 52, no. 7, pp. 1673-1682, July 2004.

Decoupling Capacitor Placement

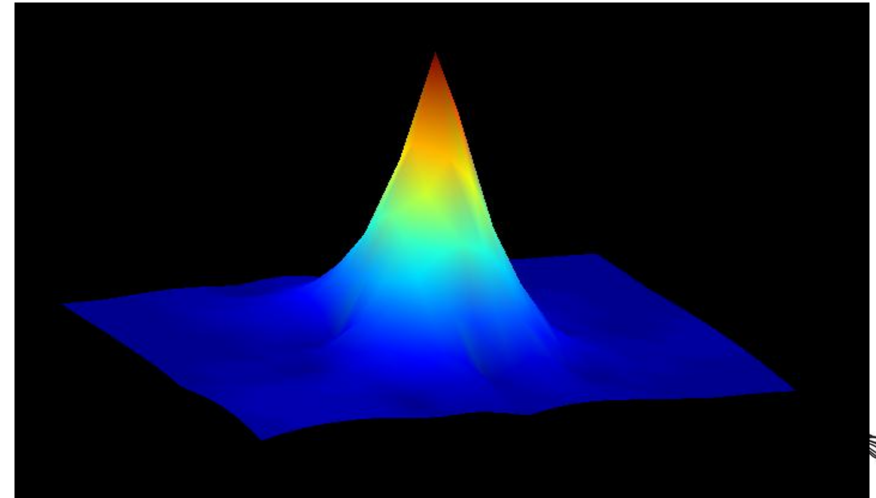




V_{peak}: 10mV

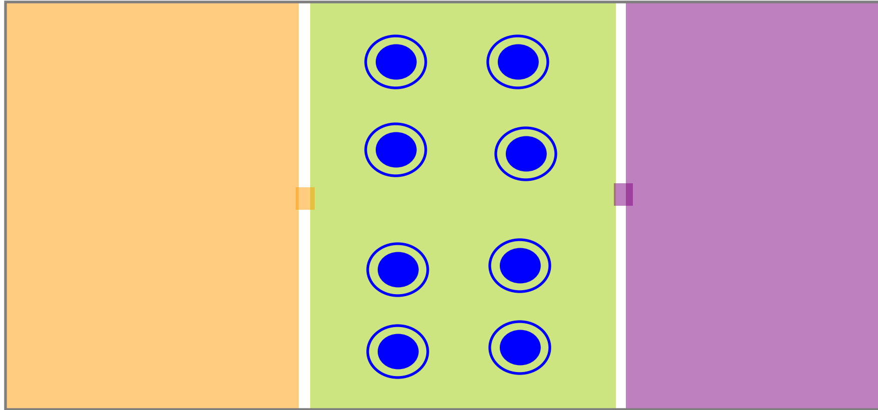


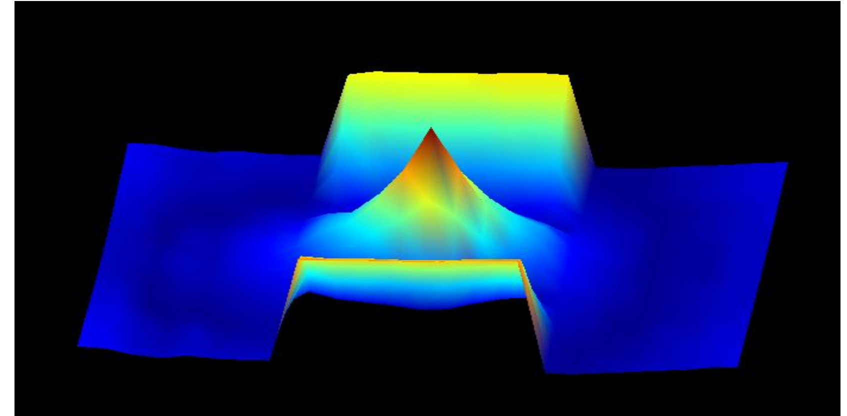
V_{peak}: 30mV



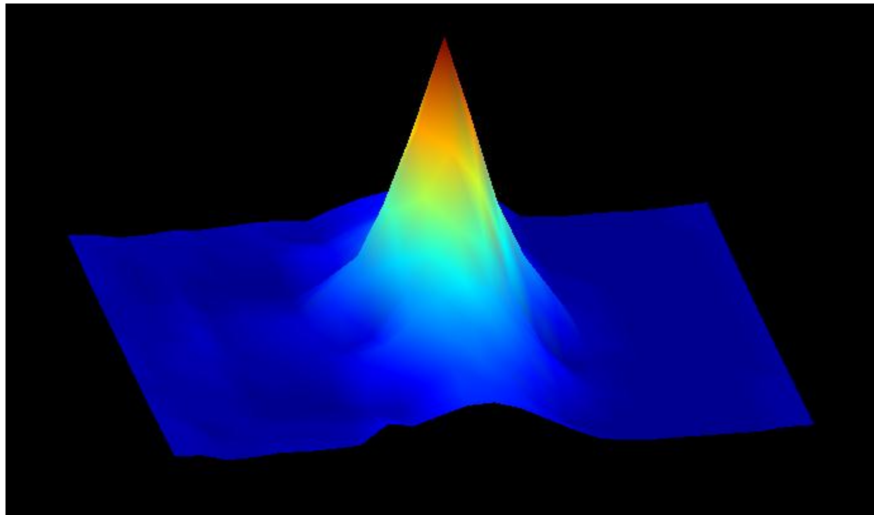
V_{peak}: 10mV (20 capacitors)

Decoupling Capacitor Placement





V_{max}=10mV; V_{analog} < 1mV



V_{peak}: 10mV

- Details of the field, current, or voltage distribution on EM structure

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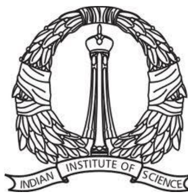
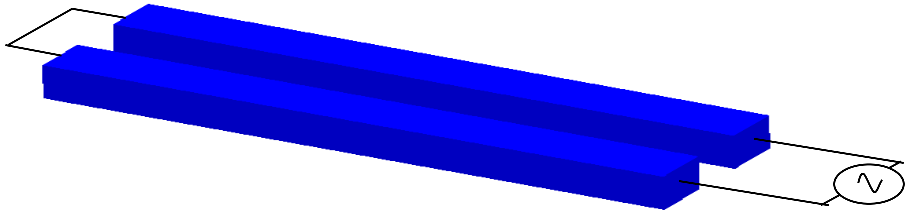
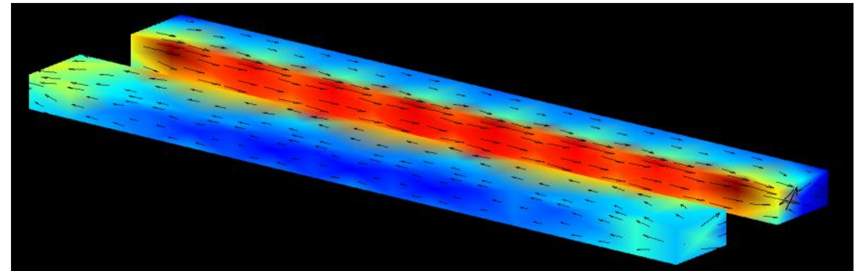
EMI/EMC

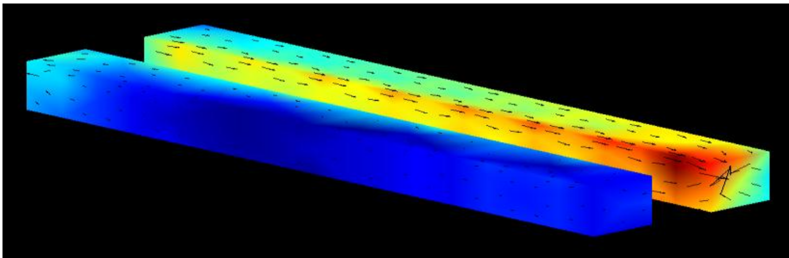
- Near electric field
- Near magnetic field

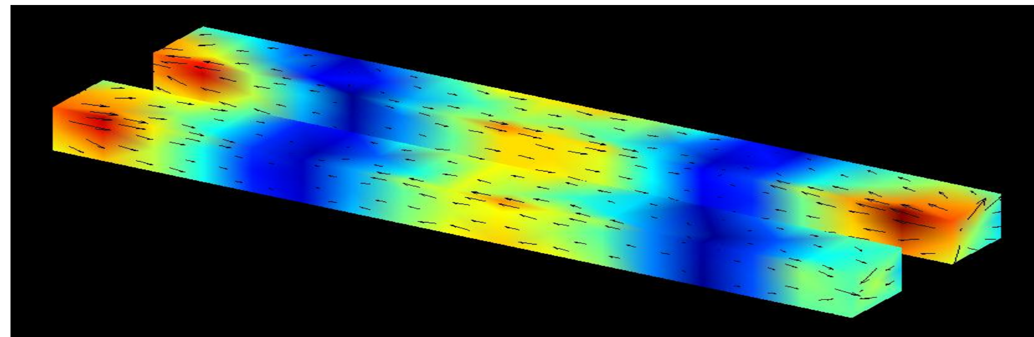


Common Mode Current





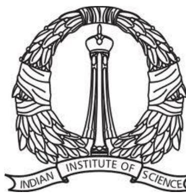




Existing Solution: Design Rule Check

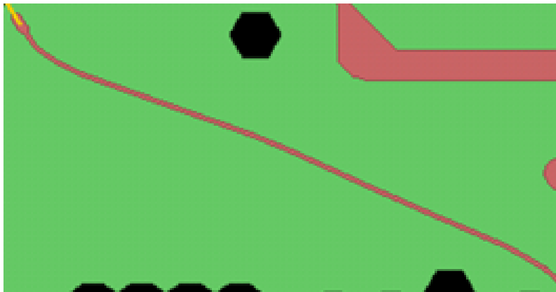
- Rule #1 – Critical next crossing gaps/slots/splits.
- Rule #2 – Parallelism/long nets coupling.
- Rule #3 – Differential pair length matching.
- Rule #4 – Differential pair return path.
- Rule #5 – Ground under clock/critical signals.
- Rule #6 – Power and ground plane separation.
- Rule #7 – Power and ground trace width.
- Rule #8 – Reference plane change.

R. Murugan, S. Chakraborty, S. Mukherjee, D. Gope, and V. Jandhyala, "Building IC-package-PCB-system EMI/EMC verification and early design flows: Challenges and methods", *Proceedings of DESIGNCON conf.,* Santa Clara, February 2010.



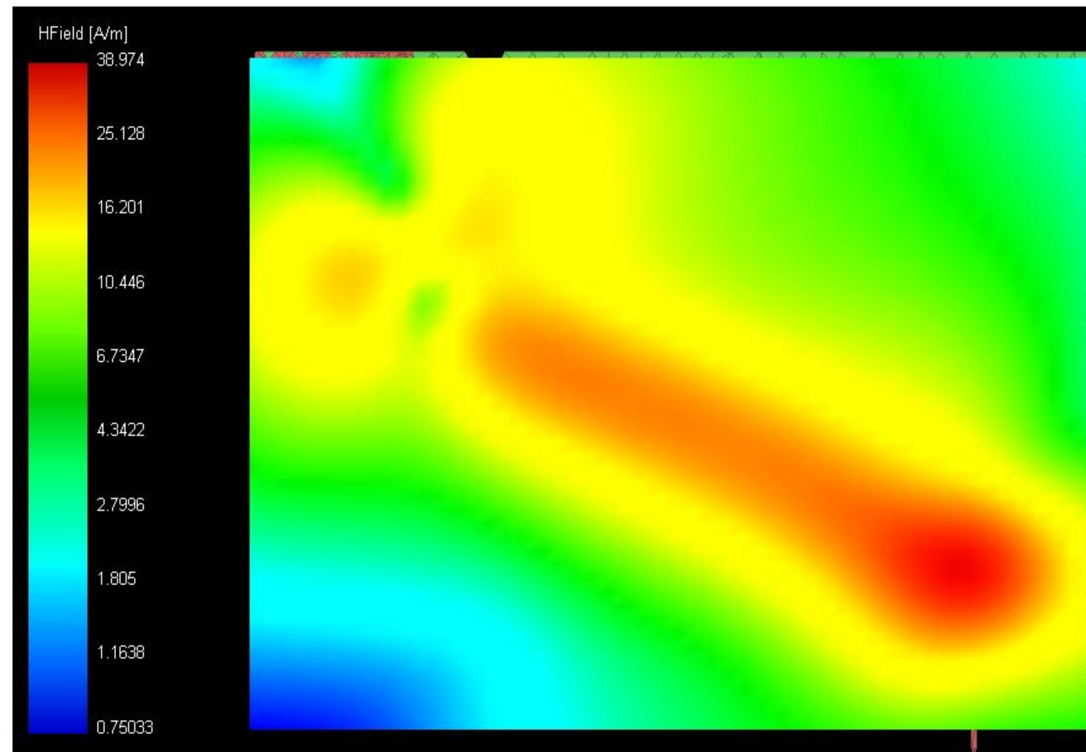
DRC Too Pessimistic

Magnetic Field: No Slots



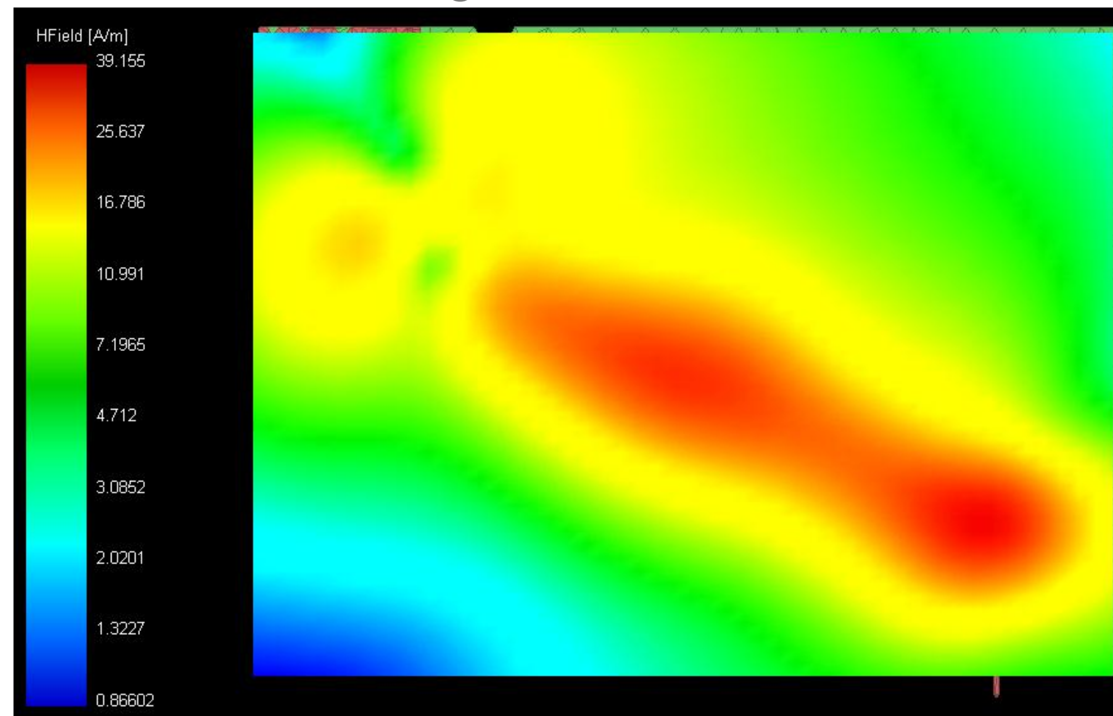
1mA Noise Current is Injected

Maximum Magnetic Field: 38.97mA/m



Magnetic Field: Longitudinal Slot

Maximum Magnetic Field: 39.15mA/m



Minimal Change in Maximum Radiation Intensity

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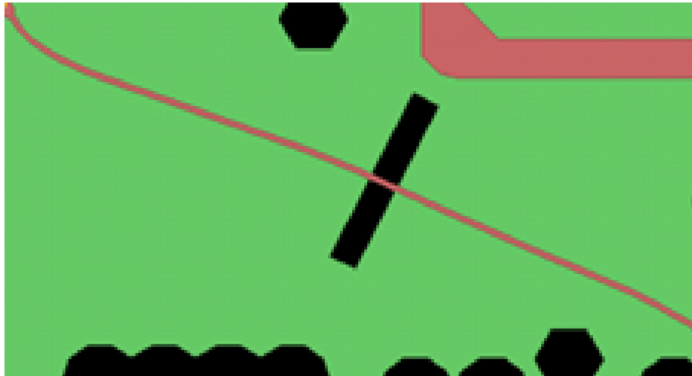
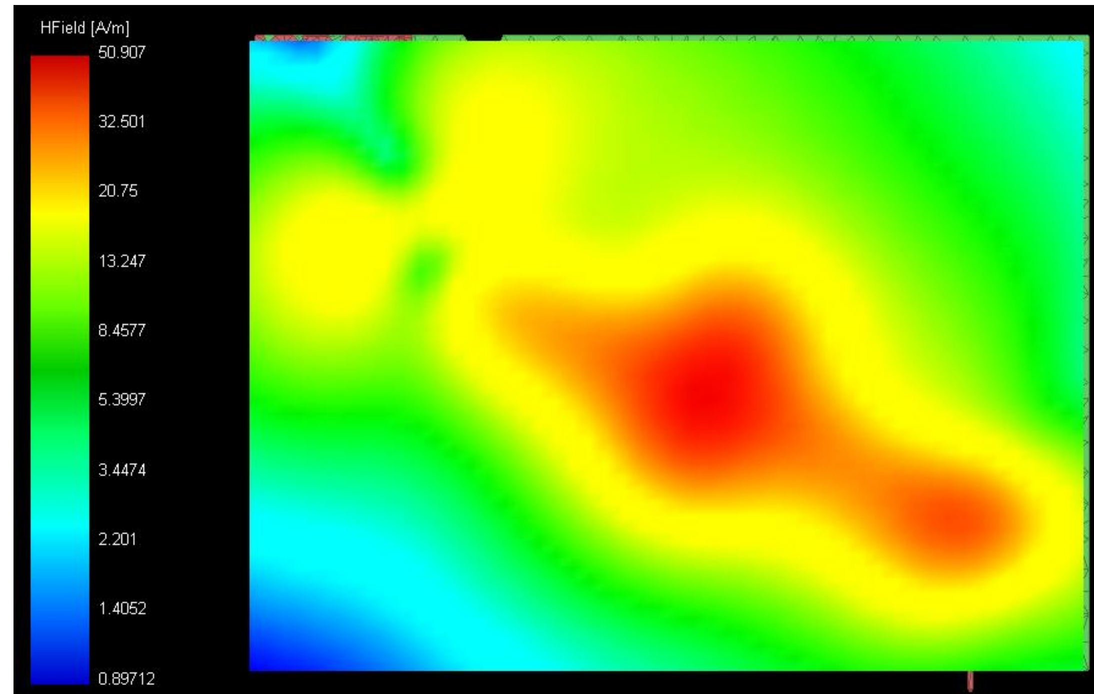
Magnetic Field: Transverse Slot



Maximum Magnetic Field: 50.9mA/m



Large Increase in Maximum Radiation Intensity

Transverse Vs Logitudinal Slots

Maximum Magnetic Field Radiation (mA/m)

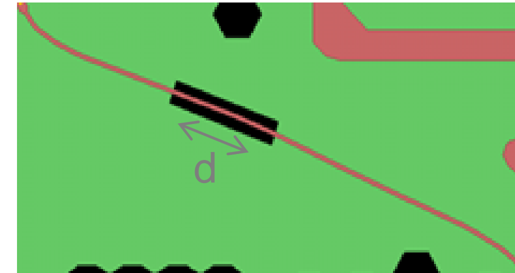
60
50
40
30
20
10
0

0 | 0.5 | 0.75 | 1 | 1.25 | 1.4 | 1.6

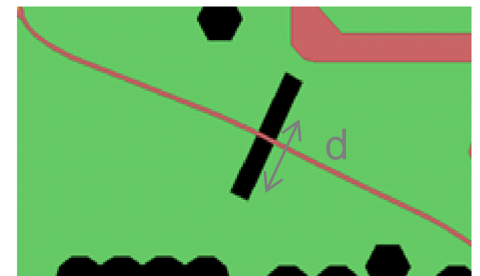
Longitudinal
Transverse

Size of the slot: d (mm)

Longitudinal



Transverse



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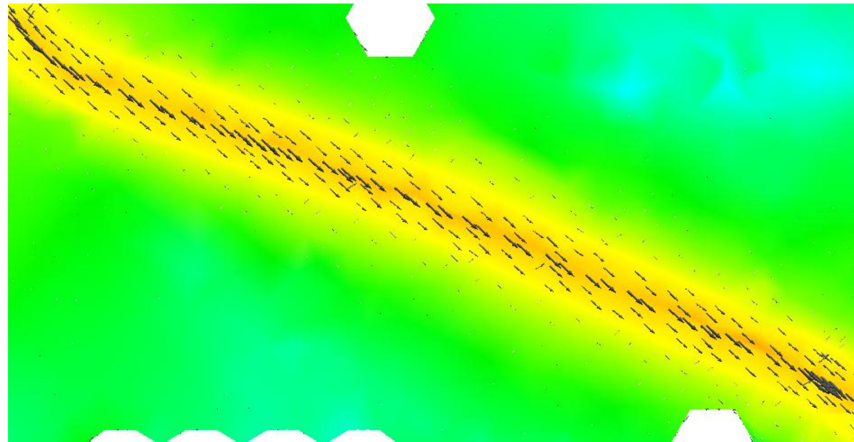
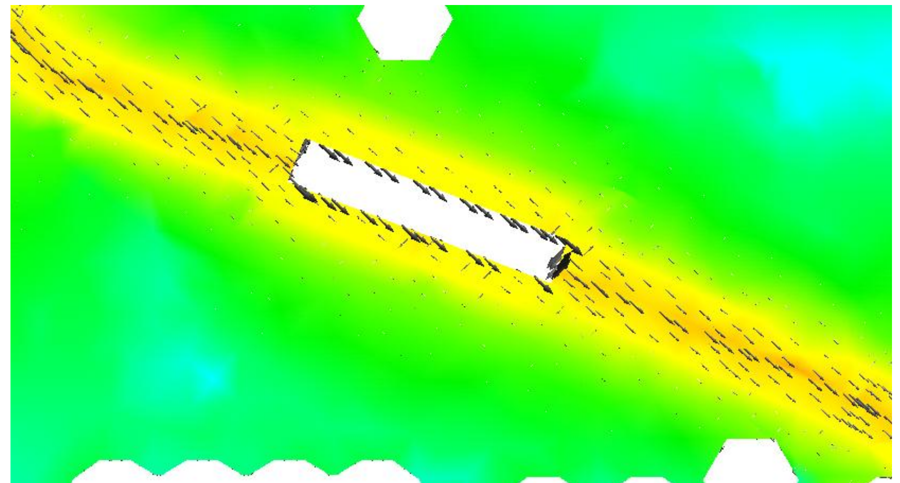
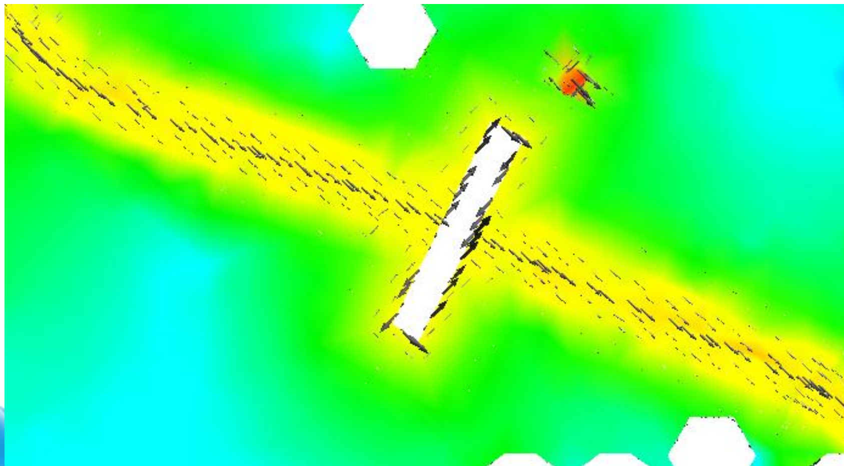
3D Fullwave Explanation



Current Density On Ground: Without Slot

Current Density On Ground: Longitudinal Slot





Current Density On Ground: Transverse Slot

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