Dipanjan Gope

Electrical Communication Engineering,
Indian Institute of Science,
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EDUCATION

Ph.D. in Electrical Engineering
University of Washington, Seattle, WA, 2005

M.S. in Electrical Engineering
University of Washington, Seattle, WA, 2003

B.Tech. in Electronics and Electrical Communications Engineering
Indian Institute of Technology, Kharagpur, India, 2000

APPOINTMENTS

Indian Institute of Science, Bangalore, India
Assistant Professor, Electrical Communication Engineering, 2011-Present

Nimbic Inc., Mountain View, USA (acquired by Mentor Graphics)
Founding member
Vice President, R&D, 2008-2011, 2013-2014
Director, R&D, 2007-2008

Intel Corp., Santa Clara, USA
Senior CAD Engineer, 2005-2007

IBM T.J. Watson Research, Yorktown Heights, USA
Technical Intern, 2004

RESEARCH AREAS

Computational Electromagnetics (EM):

The solution of Maxwell's equations for irregular 3D structures have been used traditionally for oil-exploration, detection of radar-cross-section of military vehicles, antenna analysis, bio-medical applications and more recently in predicting electrical performance of RF and high speed circuits and systems. Since 1950s applied mathematics, physics, and engineering communities have refined the EM solution using 3 fundamental analysis techniques: Finite Element Method (FEM), Finite Difference Time Domain (FDTD) method and the Method of Moments (MoM) or the Boundary Element Method (BEM). The accuracy of simulated results and the time and memory requirements are key indicators of any solution methodology. While the community has successfully addressed many challenges over the last few decades, several problems including fast direct solvers, effective full-wave preconditioners, incremental or design specific solvers remain unsolved or partially solved.

Electronic Design Automation (EDA) for high-speed chip-package-systems:

With the increasing bit rates for communication, chip-package-system level challenges like signal integrity (SI), power integrity (PI) and electromagnetic interference (EMI) play a crucial role in circuit design. RLGC parasitics or S-parameter extraction tools have been used for modeling the electromagnetic behavior of on-chip inductors and package-board interconnects using different flavors of solution methodology: 2D, 2.5D, 3D. The move towards low-cost packages with minimum layer-count, ground planes with holes, and 3D die-stacking renders a 3D treatment necessary for critical regions for accurate modeling. Therefore, the complexity of analyzing large structures like complete package and board systems with 3D accuracy presents a time and memory bottleneck. The fast solver algorithms of the last two decades have alleviated the problem at the verification stage, but the quick turn-around time required for design has been elusive. Automatic hybrid 3D-2.5D-2D formulations aided by pattern recognition may provide the incentive required for a wide-spread use of 3D tools in the design stages.

Fast iterative and direct solver algorithms:

The BEM technique uses a surface or interface mesh and gives rise to a smaller matrix size but in dense form which presents a time and memory bottleneck. In the last two decades several fast iterative solver algorithms have been devised to mitigate the problem, namely, Fast Multipole Method (FMM), low-rank based methods and Pre-corrected FFT based method. While these algorithms are capable of reducing the cost of matrix-vector products to $O(N)$ or $O(NlogN)$, the solution time is impeded by the convergence rate of the iterative solution and will require better pre-conditioning techniques particularly for full-wave applications. For the solution of very large number of right-hand-side (RHS), a different iteration-free variant of fast solvers or in other words, fast direct solvers can be very effective in expediting the matrix solution. The challenges involve reducing a traditionally $O(N^3)$ LU decomposition process to a faster linear complexity method exploiting the underlying physics of the interactions between basis functions.

Radio-Frequency (RF) sensing and inverse solvers:

RF or microwave imaging techniques, due to its non-invasive, non-ionizing, low-power and low-cost features, is amenable to regular monitoring of some diseases like breast cancer, towards early detection or post-treatment tracking. The benign-adipose and cancerous tissues exhibit different material properties, namely permittivity and conductivity in the frequency range of 100MHz to 20GHz. Given an electromagnetic field excitation, this results in different scattered fields from healthy and diseased tissues, which can be used to detect and monitor breast health. Over the last couple of decades several full-wave image reconstruction algorithms have been proposed. However, a commercial solution towards RF imaging for breast cancer detection is yet to materialize. The reason can be attributed to the computational challenges involved in the ill-posed, non-linear, inverse solution of 3D full-wave Maxwell's equations which is further exacerbated by the presence of benign fibro-glandular tissue that demonstrate low dielectric contrast with malignant tissue in the RF spectrum. The emergence of cloud computing, prominence of internet connected devices and the advances in optimization and machine learning approaches present a unique opportunity to usher in a new paradigm of personalized RF imaging sensor devices.

Antenna analysis and design:

Antennas constitute the receiver and transmitter ends for wireless communication channels. With the recent deluge in the use of mobile phones, wearable devices and in general wireless transmission, a plethora of antenna types have come to the forefront with different characteristics and application areas. The antenna properties like gain, directivity and efficiency are also dependent on the mounting structure e.g. the vehicle for military vehicular antennas and the package-board-heat-sink-chassis for those in microelectronic systems. While the field of antenna analysis is fast gaining maturity, the area of effective

antenna design or synthesis tools, particularly in the presence of mounting structures, is still at a nascent stage. Although, theoretically the design problem stands to benefit from advances in the forward analysis methodology, in reality several gaps in theory, algorithms and implementation need to be addressed before design and synthesis tools can be developed to effectively serve as suitable aid to engineers.

Parallel processing for many-core CPU, GPU, FPGA and cloud computing:

A right hand shift in the power-constrained commodity microprocessor roadmap has given rise to the many-core CPU architectures that rely on increasing the number of cores rather than clock frequency to deliver increased computing performance. Therefore, algorithms with non-trivial serial content will not scale in terms of efficiency in accordance to Amdahl's law. Consequently, fast solver algorithms of the next generation need to be amenable to parallelization and implemented with appropriate load-balancing, synchronization and cache utilization. The emergence of cloud computing and the corresponding on-demand availability of custom computing instances, also present a unique opportunity to meet the time-memory requirements and enter the magical "simulation-in-a-coffee-break" paradigm. Further, the main-streaming of GPU and FPGA processors and the increasing bus-speeds for CPU communication, may provide avenues for unprecedented speedup and memory capacity.

TEACHING:

IISc E8-202: Computational Electromagnetics (3:0) with Prof. K.J. Vinoy

- Module 1: Electromagnetic basics
- Module 2: Method of Moments
- Module 3: Finite Difference Time-Domain Method

IISc E8-262: CAD for High Speed Chip-Package-Systems (3:0)

- Module 1: Electrical Challenges in High Speed Chip-Package-Systems
- Module 2: 2D Electrical Characterization (Multiconductor Transmission lines)
- Module 3: 2.5D Electrical Characterization (Multilayered Finite-Difference Method)
- Module 4: 3D Electrical Characterization (Partial Element Equivalent Circuit Method

IISc E0-245: Android Sensor Programming (3:0)

- Module 1: Object Oriented Programing and Data Structures
- Module 2: Android Sensor Applications
- Module 3: Hybrid mobile-cloud framework

AWARDS / HONORS / ACADEMIC SERVICES

- 2015: Faculty mentor, Student Software Demonstration Prize, IEEE EPEPS, San Jose, USA
- 2015: Technical Program Committee member, IEEE SPI, Europe
- 2015-Present: Technical Program Committee member, IEEE EPEPS, USA
- 2015-Present: International Steering Committee member, IEEE EDAPS, Asia-Pacific
- 2014-2015: Technical Program Committee member, IEEE ASP-DAC, Asia Pacific
- 2014: Coauthor and advisor, Best Student Paper Award, IEEE EDAPS, Bangalore, India
- 2014: General Co-chair, IEEE EDAPS, Bangalore, India

- 2014: Technical Program Committee member, IEEE DAC, USA

- 2014: Technical Program Committee member, IEEE DATE, Europe

- 2013: Department of Science and Technology (DST) Young Scientist (Engineering Sciences)

- 2012: IEEE Senior Member

- 2012: Track chair "Interconnect and Power Networks", IEEE ICCAD

- 2010-2012: Technical Program Committee member, IEEE ICCAD

- 2008-2011: Affiliate faculty in Electrical Engineering, University of Washington

- 2006: Divisional Recognition Award for delivering signal integrity analysis for Core2 Duo, Intel

- 2003: Co-author, "best paper in session" (Mixed Signal Technology) SRC Techcon03

PUBLICATIONS

Journals:

[1] G. Chatterjee, A. Das and D. Gope, "Learning-based Fast Iterative Convergence of 3D MoM via Eigen-AGMRES Method", to appear *IEEE Transactions on Antennas and Propagation*.

[2] A. Das and D. Gope, "Adaptive Mesh Refinement for Fast Convergence of EFIE-based 3D Extraction", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, No. 3, pp. 404-414, 2015.

[3] R. Oikawa, D. Gope and V. Jandhyala, "Return-Path Extraction Technique for SSO Analysis of Low-Cost Wire-Bonding BGA Packages", *IEEE Transactions on Advanced Packaging*, vol. 2, No. 4, pp. 677-686, April 2012.

[4] V. Jandhyala, D. Gope, S. Chakraborty, R. Murugan and S. Mukherjee, "Toward Building Full-System EMI Verification and Early Design Flows Through Full-Wave Electromagnetic Simulation", International Journal of RF and Microwave Computer-Aided Engineering, vol. 22, No. 1, pp. 104-115, Dec 2011.

[5] D. Gope, A. Ruehli and V, Jandhyala, "Solving Low-Frequency EM-CKT Problems Using the PEEC Method", *IEEE Transactions on Advanced Packaging*, vol. 30, Issue 2, pp. 313-320, May 2007.

[6] D. Gope, A. Ruehli and V. Jandhyala, "Speeding up PEEC partial inductance computations using a QR based algorithm", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 15, Issue 1, pp. 60-68, Jan 2007.

[7] I. Chowdhury, S. Chakraborty, V. Jandhyala, D. Gope and J. Rockway, "A combined Circuit- Electromagnetic-Fluidic computational methodology for force prediction in Lab-On-Chip environment" *IEEE Transactions on Circuits and Systems*, vol. 53, Issue 12, pp: 2664-2672, Dec. 2006.

[8] D. Gope, A. Ruehli, C. Yang and V. Jandhyala, "(S)PEEC: Time and frequency domain surface formulation for modeling conductors and dielectrics in combined circuit electromagnetic simulations", *IEEE Transactions on Microwave Theory Tech.* vol. 54, Issue 6, Part 1, pp: 2453-2464, Jun 2006.

[9] D. Gope and V. Jandhyala, "Efficient Solution of EFIE via Low-Rank Compression of Multilevel Predetermined Interactions", *IEEE Transactions on. Antennas and Propagation,* vol. 53, Issue 10, pp. 3324 - 3333 Oct 2005*.*

[10] Dipanjan Gope and Vikram Jandhyala, "Oct-Tree Based Multilevel Low-Rank Decomposition Algorithm for Rapid 3D Parasitic Extraction", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 23, Issue 11, Nov. 2004 pp. 1575 - 1580 Nov. 2004*.*

[11] Yong Wang, Dipanjan Gope, Vikram Jandhyala and C.J. Richard Shi, "Generalized KVL-KCL Formulation for Coupled Electromagnetic-Circuit Simulation with Surface Integral Equations", *IEEE Transactions on. Microwave Theory Tech.*, vol. 52, no. 7, pp. 1673-1682, July 2004.

[12] D. Gope and V. Jandhyala, "PILOT: A Fast Algorithm for Enhanced 3D Parasitic Capacitance Extraction Efficiency", *Microwave Optical technology Letters* Vol. 41, Issue 3, pp.169-173 May 2004.

[13] V. Jandhyala, Y. Wang, D.Gope and R. Shi, "A Surface Based Integral Equation Formulation for Coupled Electromagnetic and Circuit Simulation*," Microwave Optical technology Letters*, Vol. 34, No. 2, pp. 102-106, July 2002.

Book chapter:

[1] Dipanjan Gope, Swagato Chakraborty, Vikram Jandhyala, Mosin Mondal, Woupoung Kim, Souvik Mukherjee, Rajen Murugan, and Raj Nair, in *Power Integrity Analysis and Management for Integrated Circuits*, Raj Nair and Donald Bennett, Prentice Hall Modern Semiconductor Design Series, 2010.

Conferences:

[1] A. Das and D. Gope, "Modified SPIE Formulation For Low-Frequency Stability Of Electric Field Integral Equation", to appear *Proc. IEEE Applied Electromagnetics Conference,* December 2015.

[2] G. Chatterjee and D. Gope, "Krylov Recycling Method For 3D Full-Wave EM Simulation", to appear *Proc. IEEE Applied Electromagnetics Conference*, December 2015.

[3] B. Nayak, S.V. Reddy and D. Gope, "Non-orthogonal 2.5D PEEC for Power Integrity Analysis", to appear *Proc. IEEE conference on Electrical Design of Advanced Packaging and Systems,* December 2015.

[4] N. Ambasana, G. Anand, B. Mutnury and D. Gope, "Automated Frequency Selection for Machine-Learning based EH/EW prediction from S-Parameters", to appear *Proc. IEEE conference on Electric. Perf. of Electron. Packaging*, October 2015.

[5] N. Ambasana, B. Mutnury and D. Gope, "Intelligent Rapid Investigation of S-parameters (IRIS)", (student software demonstration prize) to appear *Proc. IEEE conference on Electric. Perf. of Electron. Packaging*, October 2015.

[6] G. Chatterjee, A. Das and D. Gope, "Accelerated 3D MoM Solution of Adaptively Refined Successive New Meshes on Package-Board Geometry", to appear *Proc. IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization*, August 2015.

[7] H. Muniganti and D. Gope, "Leveraging prior state in 3-D full-wave RF imaging via Levenberg-Marquardt algorithm", *Proc. IEEE Computational Electromagnetics International Workshop (CEM)*, pp. 1-2, July 2015.

[8] A. Das and D. Gope, "A separated potential integral equation for low-frequency PMCHWT", *Proc. IEEE Computational Electromagnetics International Workshop (CEM)*, pp. 1-2, July 2015.

[9] G. Chatterjee, A. Das and D. Gope, "Fast Incremental 3D Full-Wave Analysis for Package-Board Design Iterations via Eigen-GCR", *Proc. IEEE conference on Electrical Design of Advanced Packaging and Systems*, pp. 25-28, December 2014.

[10] N. Ambasana, G. Anand, B. Mutnury and D. Gope, "Eye-Height/Width Prediction from S-Parameters using Bounded Size Training Set for ANN", (best student paper award) *Proc. IEEE conference on Electrical Design of Advanced Packaging and Systems*, pp. 17-20, December 2014.

[11] Y. Negi, N. Balakrishnan, S. M. Rao and D. Gope, "Null Field Preconditioner For Fast 3D Full-wave MoM Package-Board Extraction", *Proc. IEEE meeting on Electrical Design of Advanced Packaging and Systems*, pp. 57-60, Dec. 2014.

[12] G. Chatterjee, A. Das and D. Gope, "Fast Convergence of MoM-based Package-Board Extraction via Incremental Eigen-AGMRES Method", *Proc. IEEE meeting on Electric. Perf. of Electron. Packaging*, pp. 151-154, Oct. 2014.

[13] N. Ambasana, B. Mutnury, D. Gope and G. Anand, "Eye-Height/Width Prediction from S-Parameters using Bounded Size Training Set for ANN", *Proc. IEEE meeting on Electrical Design of Advanced Packaging and Systems*, pp. 99-102, Dec. 2014.

[14] A. Das, R. Nair and D. Gope, "Efficient Adaptive Mesh Refinement for MoM-based Package-Board 3D Full-wave Extraction", *Proc. IEEE conference on Electric. Perf. of Electron. Packaging*, pp. 239-242, October 2013.

[15] N. Ambasana, A. Chandrashekhar and D. Gope, "Application of Qualitative Imaging Methods to Electrical Performance-Aware Package Board Design", *Proc. IEEE conference on Electric. Perf. of Electron. Packaging*, pp. 247-250, October 2013.

[16] D. Gope, S. Chatterjee, D. De Araujo, S. Chakraborty, J. Pingenot and R. Camposano, "Device Physics aware 3D Electromagnetic Simulation of Through-Silicon-Vias in System Modeling", *Proc. IEEE International 3D Systems Integration Conference*, pp. 1-5, October 2013.

[17] A. Devi, M. Gandhi, K. Varghese and D. Gope, "Hardware accelerator for 3D method of moments based parasitic extraction", *Proc. IEEE symposium on Electrical Design of Advanced Packaging and Systems*, pp. 100-103, December 2013.

[18] A. Das and D. Gope, "Hybrid Aggregated-Vector Algorithm for Efficient Parallelization of Fast Multipole Method", *Proc. IEEE meeting on Electric. Perf. of Electron. Packaging*, pp. 181-184, October 2012.

[19] V. P. Padhy, N. Balarishnan, D. Gope, "Solving volume integral equation using ScaLAPACK", *Proc. Mathematical Methods in Electromagnetic Theory*, pp. 288-291, Aug. 2012.

[20] R. Camposano, D. Gope, S. Grivet-Talocia and V. Jandhyala, "Moore meets Maxwell", *Proc. IEEE Design Automation and Test in Europe*, pp. 1275-1276, 2012.

[21] R. Murugan, S. Mukherjee, M. Mi, L. Pauc, C. Girardi, D. Gope, D. de Araujo, S. Chakraborty, and V. Jandhyala, "System-level SoC Near-Field (NF) Emissions: Simulation to Measurement Correlation", Proc. Electronic Components and Technology Conference, 2012.

[22] D. Gope, V. Jandhyala, X. Wang, D. Macmillen, R. Camposano, S. Chakraborty, J. Pingenot, and D. Williams, "Towards System-Level Electromagnetic Field Simulation on Computing Clouds", *Proc. IEEE meeting on Electric. Perf. of Electron. Packaging*, pp. 167-170, October 2011.

[23] R. Oikawa, D. Gope, and V. Jandhyala, "Broadband SSO modeling for a weak signal return-path system based on the large-scale signal-power combined three-dimensional full-wave BEM solver model," *Proceedings of the IEEE Electrical Components and Technology Conference*, pp. 638-645, Las Vegas, June 2010.

[24] V. Jandhyala, S. Chakraborty and D. Gope, "Next-generation three-dimensional full-wave electromagnetic solver hybridization for large-scale signal integrity, power integrity, and EMI modeling", *Proc. International Symposium on EMC, pp. 407-412, Aug. 2010.*

[25] R. Murugan, S. Chakraborty, S. Mukherjee, D. Gope, and V. Jandhyala, "Building IC-package-PCB-system EMI/EMC verification and early design flows: Challenges and methods," *Proceedings of DESIGNCON conf.*, Santa Clara, February 2010.

[26] S. Mukherjee, D. Gope, R. Murugan, S. Chakraborty, and V. Jandhyala, "An accurate methodology for model-to-hardware calibration and correlation with PCB-package simulation using electromagnetic field solvers" *Proceedings of DESIGNCON conf.*, Santa Clara, February 2010.

[27] A.V**.** Sathanur, R. Chakraborty, V. Jandhyala, F. Ling, D. Gope and S. Chakraborty "An accurate hierarchical electromagnetic-circuit technique for statistical analysis of RF circuits**"**, *Proc. International Symposium of IEEE APS/URSI*, pp. 1-4, July 2008.

[28] Chuanyi Yang, S. Chakraborty, D. Gope and V. Jandhyala, "3D accelerated electromagnetic integral equation solvers on parallel processors for microelectronic simulation**"**, *Proc. International Symposium on EMC, pp. 539-543, Aug. 2006.*

[29] Chuanyi Yang, Dipanjan Gope and Vikram Jandhyala, "A parallel low-rank matrix compression algorithm for parasitic extraction of electrically large structures" to appear *Proc. IEEE Design Automation Conference,* pp. 1053-1056, July 2006.

[30] Vikram Jandhyala, Swagato Chakraborty, Dipanjan Gope, Chuanyi Yang, Indroneil Chowdhury and Gong Ouyang, "Accelerated, parallelized time and frequency domain simulators for complex high-speed micro-systems", *Proc*. IEEE *International Symposium of APS 2005 Conference,* pp. 123-126, 2006*.*

[31] Dipanjan Gope, Albert Ruehli and Vikram Jandhyala, "Solving Low Frequency EM-CKT Problems Using the PEEC Method", *Proc. IEEE meeting on Electric. Perf. of Electron. Packaging*, Austin, pp. 351-354, October 2005.

[32] Swagato Chakraborty, Dipanjan Gope, Gong Ouyang and Vikram Jandhyala, "Three-stage Preconditioner for Modeling Electromagnetic Components in Integrated Packages with Arbitrary Boundary Contours" *Proc. IEEE meeting on Electric. Perf. of Electron. Packaging*, Austin, pp. 199-202, October 2005.

[33] Chuanyi Yang, Swagato Chakraborty, Dipanjan Gope, Gong Ouyang and Vikram Jandhyala, "A Parallel Multilevel Low-Rank Decomposition Algorithm for Fast Simulation of High-Speed Electronic Interconnect and Packages", *Proc. IEEE meeting on Electric. Perf. of Electron. Packaging*, Austin, pp. 245-248, October 2005.

[34] Vikram Jandhyala, Swagato Chakraborty, Dipanjan Gope, and Chuanyi Yang, "Accelerating Coupled Circuit-EM Simulation in the Frequency and Time Domain", *Proc. International Symposium on IEEE EMC 2005*, vol. 3, pp 823-827.

[35] Vikram Jandhyala and Dipanjan Gope, "Fast Full-wave Electric and Magnetic Field Integral Equation Solvers based on QR Compression of Predetermined Matrices**",** *Proc. ICEEA Italy 2005*.

[36] V. Jandhyala, S. Chakraborty, D. Gope, and C. Yang, "Fast Methods for Electromagnetic and Circuit-Electromagnetic Simulation of Mixed-Signal Systems and High-Speed ICs in Time and Frequency Domains," *Proc of the 12th International Conference on Mixed Design of Integrated Circuits and Systems* (Mixdes), invited plenary talk, pp. 715-719, June 2005.

[37] Dipanjan Gope, Indranil Chowdhury and Vikram Jandhyala, "DiMES: Multilevel Fast Direct Solver Based on Multipole Expansions for Parasitic Extraction of Massively Coupled 3D Microelectronic Structures", *Proc.* IEEE *DAC Anaheim 2005 Conference*, pp. 159-162*.*

[38] Dipanjan Gope and Vikram Jandhyala, "Fast Full-wave EFIE Solution by Low-rank Compression of Multilevel Pre-determined Sub-matrices", *Proc*. IEEE *International Symposium of APS 2005 Conference,* 2005*.*

[39] Albert Ruehli, Dipanjan Gope and Vikram Jandhyala, "Mixed Volume and Surface PEEC Circuit and Electromagnetic Solver", *Proc. International Symposium on EMC Zurich 2005 Conference.*

[40] Dipanjan Gope, Albert Ruehli and Vikram Jandhyala, "Surface-based PEEC Formulation for Modeling Conductors and Dielectrics in Time and Frequency Domain Combined Circuit Electromagnetic Simulations", *Proc. IEEE meeting on Electric. Perf. of Electron. Packaging*, Boston, pp. 329-332, October 2004.

[41] Albert Ruehli, Dipanjan Gope and Vikram Jandhyala, "Block Partitioned Gauss-Seidel PEEC Solver Accelerated by QR based Coupling Matrix Compression Techniques", *Proc. IEEE meeting on Electric. Perf. of Electron. Packaging*, Boston, pp. 325-328, October 2004.

[42] Dipanjan Gope, Swagato Chakraborty and Vikram Jandhyala, "A fast parasitic extractor based on low-rank multilevel matrix compression for conductor and dielectric modeling in microelectronics and MEMS", *IEEE Design and Automation Conference,* pp. 794-799, 2004.

[43] Albert Ruehli, Dipanjan Gope and Vikram Jandhyala, "Mixed Volume and Surface PEEC Modeling", *Proc. International Symposium of IEEE APS/URSI* 2004.

[44] D.Gope and V.Jandhyala, "PILOT: A Fast Algorithm for Enhanced 3D Parasitic Capacitance Extraction Efficiency", *IEEE meeting on Electric. Perf. of Electron. Packaging*, Princeton, pp. 337-340, Oct. 2003.

[45] Yong Wang, Dipanjan Gope, Vikram Jandhyala, and C.J. Richard Shi, "Integral Equation-based Coupled Electromagnetic-Circuit Simulation in the Frequency Domain," *Proc. IEEE International Symposium of APS-URSI Ohio*, vol. 3, pp. 328-331, June 2003.

[46] Dipanjan Gope and Vikram Jandhyala, "Fast Direct Solver for Massively Coupled Parasitic Extraction Problems," *SRC TechCon Technical Digest*, Dallas, August 2003.

[47] Y. Wang, D. Gope, V. Jandhyala and C.J. Shi, "Integral Equation-based Coupled Electromagnetic-Circuit Simulation in the Frequency Domain," *SRC TechCon Technical Digest*, Dallas, August 2003.
Awarded Best Paper in Session (Mixed Signal Technology).

[48] V. Jandhyala, Yong Wang, D. Gope, S. Chakraborty and R. Shi, "A Surface-Integral Equation Based Technique for General Coupled Circuit Electromagnetic Simulation," (invited) *Proc. Progress in Electromagnetic research Symposium*, Boston, July 2002.

[49] D. Gope, S. Chakraborty, Y. Wang, Vikram Jandhyala and Richard Shi, "A Surface Based 3D Coupled Circuit Electromagnetic Simulator with Accurate Lossy Conductor Modeling," *Proc. IEEE International Symposium of APS-URSI San Antonio*, June 2002.

[50] V. Jandhyala, Y. Wang, D. Gope and R. Shi, "Coupled Electromagnetic-Circuit Simulation of Arbitrarily Shaped Conducting Structures Using Triangular Meshes," *Proc. International Symposium on Quality electronic Design*, San Jose, pp. 38-42, March 2002.

[51] Dipanjan Gope and Vikram Jandhyala, "An Iteration-Free Fast Multilevel Solver for Method of Moments Systems," *Proc. IEEE meeting on Electric. Perf. of Electron. Packaging*, Boston, pp. 177-180, October 2001.

[52] Dipanjan Gope and Vikram Jandhyala, "A Fast, Direct, Multiple Right-Hand Side Solver for the Method of Moments", *Proc. IEEE International Symposium of APS-URSI*, June 2001.

Other Articles:

[1] V. Jandhyala, D. Gope, S. Chakraborty, F. Ling, X. Wang, D. Williams and J. Pingenot, "3D Chip-Package-Board Modeling", *Printed Circuit Design and Fab.*, pp. 24-28, Nov 2008.

Patents:

[1] V. Jandhyala, S. Chakraborty and D. Gope, "Adaptive redundancy-extraction for 3D electromagnetic simulation of electronic systems", US8725484 B2, Issued May 13, 2014.

[2] V. Jandhyala, S. Chakraborty, D. Gope and F. Ling, "Mixed Decoupled Electromagnetic Circuit Solver", US20090177456 A1, Issued July 9, 2009.