A Novel All-Pass Network Implementation for Improved Group Delay Performance

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***Abstract*— In this letter, a novel all-pass network implementation is proposed using both distributed and lumped elements for high group delay. The implementation has reduced footprint and sensitivity of the group delay performance to the specified component value tolerances. It has been experimentally verified and the measured group delay is 2.4 ns at 1.85 GHz, which is thrice that reported in other approaches. The circuit finds varied applications in high resolution analog signal processing.**

***Index Terms*— All-pass network, analog signal processing, dispersive delay line, group delay dispersion.**

I. Introduction

EMERGENCE of dispersive delay lines (DDL) has led to the significant development of microwave analog signal processing (ASP) [1]–[3]. The challenges in the design of DDL is a compact, low-loss operation over broad bandwidth with high group delay dispersion (GDD). High GDD is required for high resolution ASP applications such as frequency discriminator [2] and compressive receiver [4]. However, there are only a few DDL technologies with high GDD at radio frequencies (RF), providing new research opportunities.

All-pass networks (APN) have been explored as a potential DDL technology owing to its independent control over the magnitude of loss characteristics and dispersion in group delay response [1] [5]. Second order APN is characterised by two design parameters, resonance frequency f_r and coefficient k, lying in the range 0 to 1 and determining the peak group delay [6]. Peak group delay of APN is obtained at f_r, and can be increased by a lower coefficient k [6]. APN has been implemented using distributed components as commensurate and non-commensurate C-sections [1]. Peak group delay achieved using single stage C-section implementation at ultra-high frequencies (UHF) is in range of hundreds of ps. Several stages of these have to be cascaded to obtain high GDD (low k), leading to a large device footprint. Microstrip-slotline open stub with conventional and deformed stub designs [3] [7] has been proposed as an alternative to obtain high group delay and lower device footprint. However, even these have a peak value under 1 ns. On the other hand, lumped implementations of APN in [2] [5] using surface mount devices (SMD) (0402 package) can provide high GDD for sub GHz frequencies. As reported in [6], low k ($\approx$ 0.1) APN design at UHF leads to high range of inductor and capacitor values, causing considerable problems in implementation as they are at fabrication extremities. Network transformations are carried out [6] to reduce the range of component values. However, the number of components in each stage increases, thereby increasing the assembly loss, Q factor loss and sensitivity to component value tolerances.

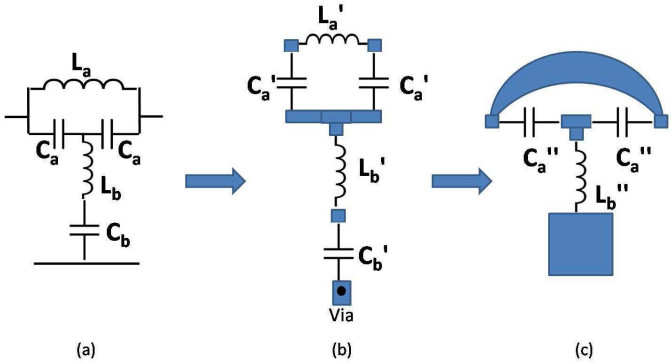

Fig. 1. All-pass network, bridged-T topology using (a) ideal components (b) co-simulation layout with SMD components (c) proposed design

To overcome the above limitations, a novel implementation of APN using both distributed and lumped elements is proposed for a high group delay at UHF. Sensitivity analyis is carried out for all components within the tolerance limits of the lumped SMD APN design [8] and the more sensitive components are replaced by board level implementations [9]. Measured results are presented to validate the design. The APN presented serves as a building block for high resolution ASP applications.

II. All-Pass Network

All-pass network (APN) is designed for $f_r = 1.8$ GHz and peak group delay $\tau = 2.4$ ns. The coefficient k is obtained as 0.1474 [6] [10]. Bridged-T equalizer network shown in Fig. 1(a) is chosen for implementation, as it has the least number of components among all the lumped APN topologies [10]. Component values for the same are obtained as $L_a = 1.3033$ nH, $C_a = 11.997$ pF, $L_b = 14.997$ nH and $C_b = 0.53290$ pF [10]. The group delay response using the ideal component values is shown in Fig. 2(a).

A. Limitations of Implementation Using SMD Components

Co-simulation design procedure in [5] is employed to analyse the APN considering parasitic effects of mounting

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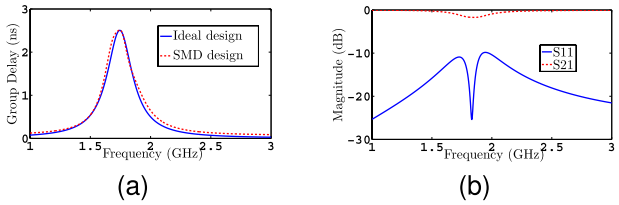

Fig. 2. Co-simulation design using SMD components (a) Group delay (b) S-parameters

TABLE I
COMPONENT DETAILS OF LUMPED SMD DESIGN

Component	Value	Q factor @900 MHz	SRF (GHz)	Tolerance
L'_a	1.4 nH	29	6	$\pm$0.2 nH
C'_a	9 pF	500	2.5	$\pm$0.1 pF
L'_b	12 nH	50	3.5	$\pm$5%
C'_b	0.5 pF	600	10	$\pm$0.1 pF

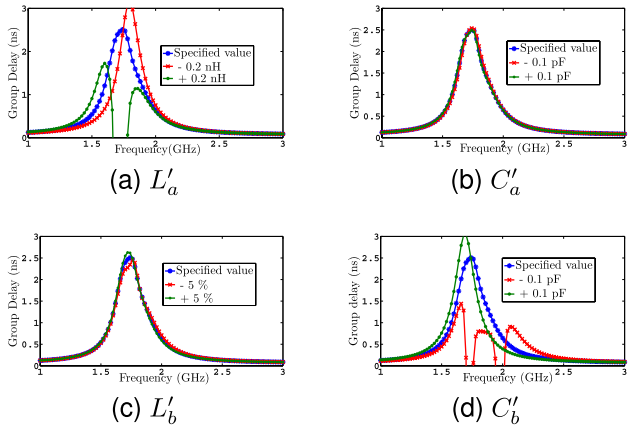

Fig. 3. Lumped SMD design: Group delay sensitivity within specified tolerance of individual components

pads, component value availability, finite Q factor, self resonance frequency (SRF) and tolerance of the individual components. The closest available component values along with their technological limitations from the datasheet are tabulated in Table I. The CBR series capacitor from Kemet Corporation and 744 765A series inductor from Wurth electronics are considered. The layout is shown in Fig. 1(b). The group delay and S-parameter performance is shown in Fig. 2.

The Q factor of the chosen components has negligible effect on the group delay response and affects only the loss characteristics [5]. Therefore, SMD components based design on printed circuit board (PCB) is analyzed for the performance variation within the component tolerances. From DDL performance point of view, changes observed in group delay response due to tolerance is more pronounced than in the magnitude of S -parameters. The group delay sensitivity is shown in Fig. 3.

It can be observed from Fig. 3(a) and 3(d) that component variation of L'_a and C'_b within the specified tolerance limits greatly affects the group delay response. Therefore, L'_a and C'_b are replaced by distributed implementations and the design procedure is shown in the following subsection. It should also

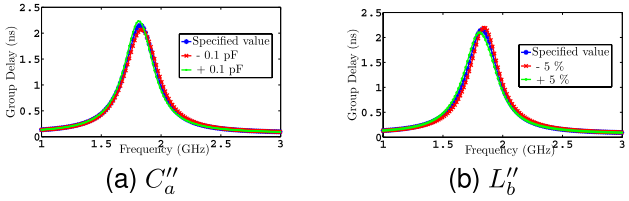

Fig. 4. Proposed design: Group delay sensitivity within specified tolerance of individual components

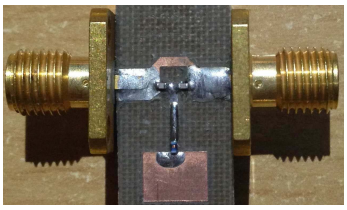

Fig. 5. Photograph of the fabricated hardware

be noted from Table I that the SRF of C'_a is very close to the frequency f_r of 1.8 GHz.

B. Proposed Design

The bridged-T circuit topology is divided into series and parallel resonance branches [10]. The inductor L_a is replaced by a small section of transmission line and the capacitor C'_a is tuned such that the series resonance is matched to that of the ideal design. The capacitor C_b is replaced by a parallel plate patch capacitor. Considering the C''_a value obtained and the patch capacitor, the inductor L''_b on the shunt line is tuned to match the parallel resonance to the ideal design. The circuit model thus designed is shown in Fig. 1(c). The resonance matching can be observed in the behaviour of the imaginary part of impedances of ideal and proposed design, as the imaginary part changes the polarity at the resonance frequency.

The design and analysis is carried out in advanced design system (ADS2015) using finite element method (FEM) solver. The effect of SRF is captured by adding the parasitic model of the individual lumped components, making it close to the practical circuit. The values of L''_b and C''_a are varied within the specified tolerance limits of the components. It can be observed from Fig. 4 that the group delay response has very low sensitivity to component value variation.

III. FABRICATION AND TESTING

To validate the proposed APN design in Section II-B, a hardware prototype is developed. The design was fabricated on Arlon AD250 substrate ($\epsilon_r = 2.5$, $h = 62$ mil, $\tan\delta = 0.0018$). The SMD components have 0402 package and their details are given in Table II. Fig. 5 shows the photograph of the fabricated hardware.

The S-parameters and group delay were measured using vector network analyzer PNA-N5320A from Keysight technologies. The measured maximum insertion loss and minimum return loss of the circuit are 2 dB and 12.75 dB and the performance over the band is shown in Fig. 6(a). The group

TABLE II
COMPONENT DETAILS OF THE PROPOSED DESIGN

Component	Value	Q factor @900 MHz	SRF (GHz)	Tolerance	Model	Vendor
C_a''	4 pF	500	4.05	±0.1 pF	CBR04C 409B1GAC	Kemet Corporation
L_b''	6.8 nH	50	5.3	±5%	744765 068A	Wurth Electronics

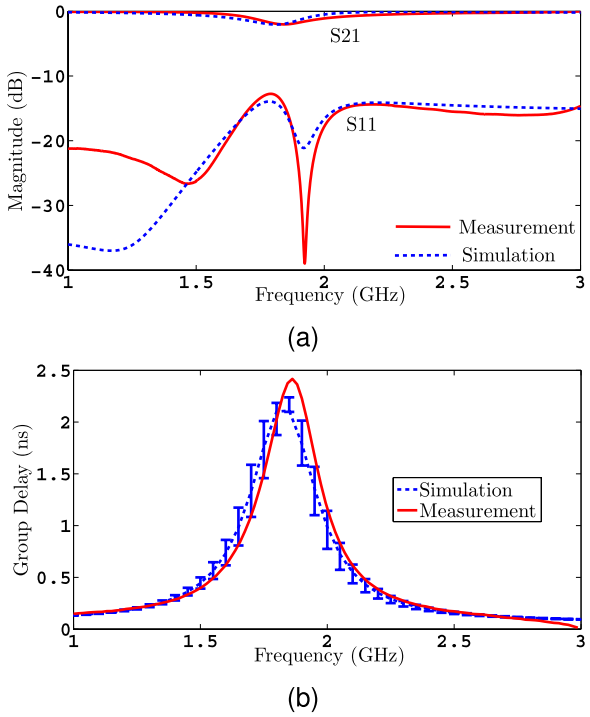

Fig. 6. Proposed design: FEM co-simulation and measurement comparison (a) S-parameters (b) Group delay

TABLE III
PERFORMANCE SUMMARY

Technology	Group Delay peak (ns)	f_r (GHz)	S21 (dB)	Device footprint (mm*mm)
Complementary slot-stub [3]	0.5	2.5	0.5	39*43
Complementary deformed structure [7]	0.8	2.5	0.9	18*35
Proposed APN	2.4	1.85	2	10*15

delay response is shown in Fig. 6(b). It is compared to the simulation result along with an error margin that corresponds to the maximum tolerance indicated by both Fig. 4(a) and 4(b). The marginal difference in the group delay response can be attributed to parasitic modeling and connector bulkhead effects. The performance summary of different DDL technologies using APN is given in Table III.

It can be noted from Table III that the peak group delay achieved using the proposed approach is thrice that reported in other APN implementations. The device footprint is only $1/4^{th}$ of other topologies, and can be further reduced by using other substrates. The proposed design approach is scalable to other frequencies, and these will only be limited by the SRF of available SMD components. Although the insertion loss is marginally higher, this is normally not a major issue and can be compensated by the gain of active circuits in a system when required.

IV. CONCLUSION

In this work, an all-pass network is presented with a novel board level implementation for high group delay, consisting of both lumped SMD components and distributed elements. The maximum group delay achieved is 2.4 ns at 1.85 GHz. The added advantages of the proposed design are reduced device footprint and lower group delay sensitivity to component value tolerances. The implementation is attractive in practical applications as it is a single layer microstrip realisation with less complex fabrication procedure and fewer components to integrate.

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