Hardware-Efficient FPGA Implementation of OTSM Transceiver for High-Mobility 6G Communications

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***Abstract*—Orthogonal Time Sequency Multiplexing (OTSM) has emerged as a high-performance single-carrier modulation paradigm specifically engineered to mitigate the severe doubly-selective fading inherent in high-mobility wireless channels. By multiplexing information symbols in the delay-sequency (DS) domain, OTSM achieves superior robustness against high Doppler shifts compared to traditional multi-carrier and frequency-domain schemes. This paper presents a high-throughput, multiplier-less FPGA-based transceiver architecture for OTSM, designed to bridge the gap between theoretical gains and real-time physical-layer realization. A core innovation is the replacement of computationally intensive Fast Fourier Transform (FFT) stages with hardware-efficient Walsh Hadamard Transform (WHT) modules. By leveraging the dyadic properties of the DS domain, the proposed design eliminates the need for complex-valued multiplications, significantly reducing arithmetic complexity and power consumption. The architecture features a fully pipelined data path encompassing symbol mapping, circular interleaving, and zero-padding, which achieves substantial reductions in logic-gate utilization and computational latency. Synthesis results on a Xilinx FPGA platform validate the feasibility of OTSM for low-latency, high-velocity communication links, offering a scalable and hardware-efficient blueprint for B5G/6G waveform implementations.**

***Index Terms*—OTSM, WHT, OTFS, FFT, FPGA, Sequency**

I. Introduction

Orthogonal Time Sequency Multiplexing (OTSM) has recently emerged as a robust single-carrier modulation candidate specifically tailored for high-mobility wireless communications. Unlike conventional multi-carrier systems, OTSM arranges information symbols within the delay-sequency (DS) grid, where "sequency" denotes the normalized rate of zero crossings per unit time [1]. This domain offers a unique advantage in doubly-selective channels characterized by high Doppler spreads and significant multipath- as it exploits the sparse representation of the channel impulse response. In the OTSM framework, data blocks are precoded using the Walsh Hadamard Transform (WHT), an orthogonal transformation that maps symbols onto a set of basis functions consisting of rectangular pulses. This is followed by a row-column interleaving process that effectively distributes the symbol energy across the time-sequency plane, thereby extracting full transmit diversity [1], [2].

The OTSM transmitter architecture performs multiplexing through a cascaded operation of Time-Division Multiplexing (TDM) and Walsh-Hadamard Sequency Multiplexing. The input symbol matrix $\mathbf{X} \in \mathbb{C}^{M \times N}$ undergoes a two-step transformation: first, a row-column interleaver decorrelates the symbols against localized channel fades; second, an Inverse WHT (IWHT) is applied along the sequency dimension. This mapping ensures that each data symbol is spread across the entire sequency bandwidth, providing inherent robustness against frequency-selective fading. To prevent Inter-Block Interference (IBI) arising from the delay spread of the channel, Zero-Padding (ZP) or Cyclic Prefix (CP) is appended, ensuring the circularity of the convolution in the DS domain [3], [4].

At the receiver, the duality of the WHT is leveraged to demultiplex the sequency components. Because the WHT basis functions are inherently orthogonal and binary-valued (± 1), the detection process avoids the complex transcendental multiplications required by the Fast Fourier Transform (FFT). This allows for the deployment of low-complexity Single-Tap Minimum Mean Square Error (MMSE) equalization or advanced iterative interference cancellation (IC) detectors. In highly dispersive channels, these sequency-domain detectors demonstrate performance parity with Orthogonal Time Frequency Space (OTFS) systems but at a fraction of the computational overhead [3]. Despite the theoretical promise of D-S domain processing, the transition to physical-layer realization requires a hardware-centric validation. Field Programmable Gate Arrays (FPGAs) serve as the definitive platform for such high-speed digital signal processing due to their deterministic latency and massive spatial parallelism. While OTFS relies on complex-valued FFT operations that consume significant Digital Signal Processing (DSP) slices and memory bandwidth, OTSM's reliance on the WHT suggests a path toward "multiplier-less" architectures.

In this work, a high-throughput FPGA implementation of a complete OTSM transceiver is presented. The proposed architecture replaces traditional FFT-based stages with optimized, pipelined WHT modules, significantly reducing the logic-gate footprint and power consumption. We detail the hardware mapping of the symbol interleaver, the dyadic WHT processing core, and the synchronization mechanisms. Synthesis results and hardware-in-the-loop (HIL) simulations demonstrate that the proposed design achieves a superior balance between throughput and resource utilization, confirming OTSM as a hardware-efficient waveform for B5G and 6G high-mobility scenarios.

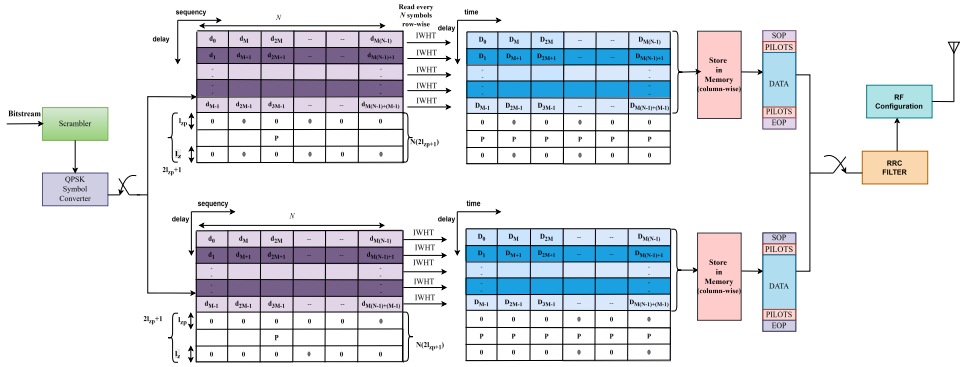

Fig. 1. FPGA based transmitter architecture for OTSM.

II. OTSM System Model

A. Transmitter and Receiver Operation

The transmitted OTSM signal frame has a total duration of $T_f = NT$ and occupies a total bandwidth of $B = M\Delta f$, where variables N is the total number of time slots which is selected as a power of two, T is the time duration of a single pulse or symbol, M is the total delay samples and Δf represents the frequency deviation. We assume the condition $T\Delta f = 1$, which implies that the OTSM signal is critically sampled regardless of the pulse shaping waveform employed. The operational structure of the OTSM transceiver is illustrated in Fig. 1.

1) Transmitter: The input bit stream is first randomized via a scrambler, and the resulting sequence is mapped to QPSK symbols $\mathbf{x} = [\mathbf{x}_0^T, \mathbf{x}_1^T, \ldots, \mathbf{x}_{M-1}^T]^T$. These symbols are grouped into column vectors $\mathbf{x}_m \in \mathbb{C}^{N\times 1}$ and arranged into a matrix $\mathbf{X} \in \mathbb{C}^{M\times N}$ to form the delay–sequency grid:

$$\mathbf{X} = [\mathbf{x}_0, \ldots, \mathbf{x}_{M-1}]^T. \tag{1}$$

The final $L_{\max}$ symbol vectors, specifically $\mathbf{x}_m$ for $m \geq M - L_{\max}$ (where $L_{\max}$ denotes the discrete channel delay spread index), are set to zero. As shown in Fig. 1, this Zero Padding (ZP) is applied in the delay domain to mitigate inter-block interference (IBI) caused by the channel delay spread.

An N-point Walsh-Hadamard Transform (WHT) is then performed on each symbol vector to transform the signal representation from the delay–sequency domain to the delay–time domain:

$$\tilde{\mathbf{X}} = \mathbf{X}\mathbf{W}_N. \tag{2}$$

The matrix $\tilde{\mathbf{X}}$ contains the delay–time domain samples, which are vectorized to form the time-domain sample vector $\mathbf{u} \in \mathbb{C}^{NM\times 1}$ for transmission through the physical channel:

$$\mathbf{u} = \mathrm{vec}(\tilde{\mathbf{X}}). \tag{3}$$

The transmitter operation can be expressed in a consolidated matrix form as:

$$\mathbf{u} = \mathbf{K}(\mathbf{I}_M \otimes \mathbf{W}_N)\mathbf{x}, \tag{4}$$

where $\mathbf{K}$ is the row–column interleaver matrix. This permutation is known as a *perfect shuffle* and satisfies the following property for square matrices $\mathbf{A}$ and $\mathbf{B}$:

$$(\mathbf{A} \otimes \mathbf{B}) = \mathbf{K}(\mathbf{B} \otimes \mathbf{A})\mathbf{K}^T. \tag{5}$$

Since $\mathbf{K}$ is a permutation matrix, $\mathbf{K}^{-1} = \mathbf{K}^T$. By applying the perfect shuffle property to (4), the transmitter operation is redefined as:

$$\mathbf{u} = (\mathbf{W}_N \otimes \mathbf{I}_M)(\mathbf{K}\mathbf{x}). \tag{6}$$

The resulting samples are pulse-shaped, converted from digital to analog, and transmitted as a continuous-time signal $u(t)$.

2) Receiver: At the receiver, the incoming signal $v(t)$ is processed by the RF front-end and converted into a digital signal via analog-to-digital conversion (ADC). The resulting time-domain samples are collected into a vector $\mathbf{v} \in \mathbb{C}^{NM\times 1}$. These samples are rearranged column-wise into a matrix $\tilde{\mathbf{Y}} \in \mathbb{C}^{M\times N}$, yielding the delay–time domain representation:

$$\tilde{\mathbf{Y}} = \mathrm{vec}^{-1}_{N,M}(\mathbf{v}). \tag{7}$$

The received information symbols are obtained by applying an N-point WHT to the delay–time samples:

$$\mathbf{Y} = [\mathbf{y}_0, \mathbf{y}_1, \ldots, \mathbf{y}_{M-1}]^T = \tilde{\mathbf{Y}}\mathbf{W}_N. \tag{8}$$

The receiver operation can be expressed in consolidated matrix form as:

$$\mathbf{y} = (\mathbf{I}_M \otimes \mathbf{W}_N)(\mathbf{K}^T\mathbf{v}), \tag{9}$$

where $\mathbf{y} = [\mathbf{y}_0^T, \mathbf{y}_1^T, \ldots, \mathbf{y}_{M-1}^T]^T$ represents the vector of estimated information symbols.

B. Input-Output Relation

Starting from the received time-domain signal $v(t)$, the continuous-time input-output relation is given by:

$$v(t) = \int_0^{\tau_{\max}} g(\tau, t)u(t-\tau)\,d\tau + n(t), \tag{10}$$

where $g(\tau, t)$ is the time-varying channel impulse response and $n(t)$ represents additive white Gaussian noise (AWGN). At the receiver, the signal is baseband down-converted and sampled at intervals $T_s = \frac{T}{M}$. The discrete-time input–output relation is expressed as:

$$\mathbf{v} = \mathbf{G}\mathbf{u} + \mathbf{w}, \tag{11}$$

where $\mathbf{G} \in \mathbb{C}^{NM\times NM}$ is the time-domain discrete baseband channel matrix and $\mathbf{w}$ is the sampled noise vector. Substituting the transmitter and receiver definitions from (6) and (9) into (11), the relation in the delay-sequency domain is:

$$(\mathbf{W}_N \otimes \mathbf{I}_M)(\mathbf{K}\mathbf{y}) = \mathbf{G}(\mathbf{W}_N \otimes \mathbf{I}_M)(\mathbf{K}\mathbf{x}). \tag{12}$$

By reversing the transmitter operations, the input–output relation can be represented in terms of information symbols as:

$$\mathbf{y} = \mathbf{H}\mathbf{x} + \tilde{\mathbf{w}}, \tag{13}$$

where the effective delay–sequency channel matrix $\mathbf{H}$ and the filtered noise $\tilde{\mathbf{w}}$ are defined as:

$$\mathbf{H} = (\mathbf{I}_M \otimes \mathbf{W}_N)(\mathbf{K}^T \mathbf{G} \mathbf{K})(\mathbf{I}_M \otimes \mathbf{W}_N), \tag{14}$$

$$\tilde{\mathbf{w}} = (\mathbf{I}_M \otimes \mathbf{W}_N)(\mathbf{K}^T \mathbf{w}). \tag{15}$$

The bandwidth of the matrix $\mathbf{G}$ is $L_{\max} + 1$, where each row contains at most L non-zero elements corresponding to the distinct delay taps. As illustrated in Fig. 1, the null symbols in the delay sequency domain serve as interleaved guard bands in the time domain, effectively preventing inter-block interference. Consequently, the strictly upper triangular components of the time-domain channel matrix can be neglected in the zero-padded OTSM framework.

III. Implementation of OTSM Transceiver

A. OTSM Frame Architecture

Fig 3 shows the frame structure used in the proposed OTSM system consists of several fields that helps in synchronization, channel estimation, and reliable data transmission. The main components of the frame include the Start of Frame (SOF), pilot symbols, Start of Message (SOM), and the data payload.

1) Start of Frame (SOF): The Start of Frame (SOF) marks the beginning of every transmitted frame. This field is used by the receiver to detect the arrival of a new frame and achieve proper synchronization with the incoming signal. The SOF usually consists of a predefined sequence known to both the transmitter and receiver. By correlating the received signal with this known sequence, the receiver can identify the frame boundary and align the processing stages correctly.

2) Pilot Symbols: Pilot symbols are inserted after the SOF to assist in channel estimation and system calibration. These symbols are known reference signals transmitted along with the data. At the receiver, the pilot symbols are compared with their known transmitted values to estimate the channel characteristics such as delay, Doppler shift, and fading effects. Accurate channel estimation helps improve symbol detection and reduces the error rate in the communication system.

3) Start of Message (SOM): The Start of Message (SOM) field indicates the beginning of the actual information payload within the frame. It acts as a marker that separates the control and synchronization fields from the data symbols. Once the receiver detects the SOM, it begins processing the subsequent symbols as part of the message data. This helps maintain a clear boundary between synchronization information and the transmitted data.

4) Data Payload: The data field contains the actual information symbols that need to be transmitted through the OTSM system. These symbols are generated from the input bitstream after QPSK modulation. The modulated symbols are arranged on the delay–Sequency grid and further processed through the IWHT and OFDM modulation stages before transmission. At the receiver, the reverse processing operations are applied to recover the transmitted data symbols and reconstruct the original bitstream.

The combination of SOF, pilot symbols, SOM, and data payload ensures reliable communication by enabling proper synchronization, channel estimation, and accurate data detection within each transmitted frame.

This frame structure allows the receiver to correctly detect the start of the transmission and process the incoming symbols in an organized manner.

B. OTSM Transceiver Implementation Architecture

The hardware implementation of the Orthogonal Time Sequency Multiplexing (OTSM) transceiver follows a structured, pipelined signal processing chain designed for deterministic latency and high throughput on an FPGA platform. The architecture is partitioned into two primary subsystems: the digital baseband transmitter and the corresponding receiver.

1) Transmitter Architecture: The transmitter processes the incoming bitstream through a hardware-optimized scrambler to randomize data sequences, thereby mitigating long repetitive patterns and enhancing the spectral properties of the waveform. The randomized bits are mapped onto a QPSK constellation, where bit-pairs are converted into complex-valued in-phase (I) and quadrature (Q) components. These symbols are organized into a two-dimensional $\mathbf{X} \in \mathbb{C}^{M \times N}$ grid within the delay-sequency (DS) domain, where rows and columns represent the delay and sequency dimensions, respectively.

To suppress Inter-Block Interference (IBI) induced by multipath propagation, Zero Padding (ZP) is appended based on the maximum channel delay spread $\tau_{\max}$. The core of the OTSM modulation involves the application of an Inverse Walsh-Hadamard Transform (IWHT) along the sequency dimension. Unlike the FFT, the IWHT utilizes binary basis functions, which are implemented in hardware using a multi-stage butterfly architecture consisting exclusively of additions and subtractions. This operation maps the sequency symbols to the delay-time domain, spreading the energy of each information symbol across the temporal block to provide inherent Doppler resilience.

The resulting delay-time samples are stored in a dual-port RAM and serialized through a column-wise readout mechanism. Prior to pulse shaping, the architecture inserts a pilot-aided frame structure consisting of start-of-packet (SoP) pilots, data symbols, and end-of-packet (EoP) markers to facilitate synchronization and channel tracking. Finally, a Root Raised Cosine (RRC) FIR filter performs pulse shaping to constrain the occupied bandwidth and minimize Inter-Symbol Interference (ISI) before the samples are passed to the RF front-end for upconversion.

2) Receiver Architecture: At the receiver, the incoming signal is downconverted and processed by a matched RRC filter. A dedicated Start-of-Frame (SoF) Detection unit monitors the incoming stream for the known pilot sequence to establish temporal synchronization. The synchronized samples are written column-wise into a two-dimensional memory buffer to reconstruct the delay–time grid.

The demultiplexing process is initiated by applying a forward WHT along the time dimension, recovering the symbol structure in the delay sequency domain. To counteract

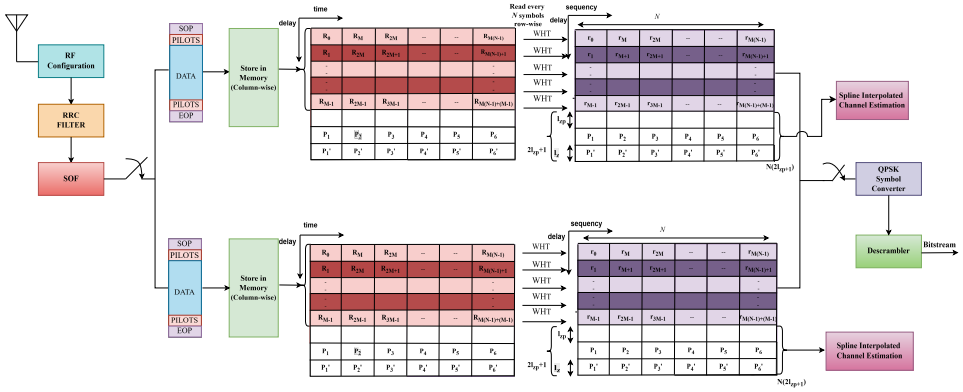

Fig. 2. FPGA based receiver architecture for OTSM.

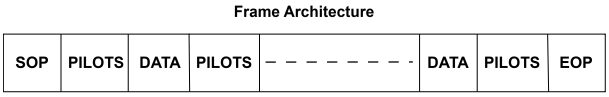

Fig. 3. OTSM Frame Architecture

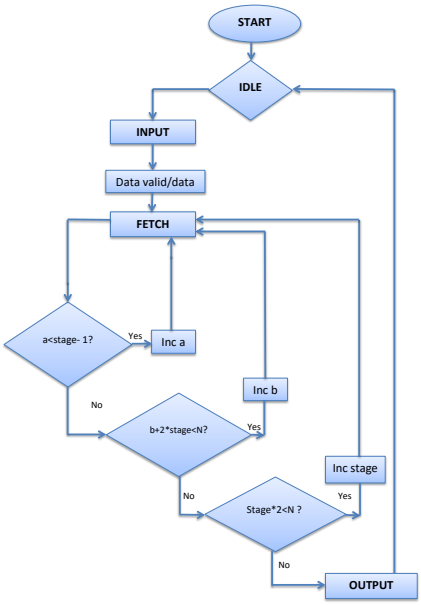

Fig. 4. Flowchart of WHT

the doubly-selective fading of the wireless channel, Spline Interpolation-based Channel Estimation is implemented. This module utilizes the embedded pilot symbols to compute a high-resolution estimate of the channel impulse response across the DS grid.

Channel equalization is performed using the estimated coefficients to mitigate the effects of delay-Doppler spreading. The equalized complex symbols are processed by a QPSK demapper, which translates constellation coordinates back into binary data. Finally, the hardware descrambler restores the original bit sequence. The resulting architecture leverages the computational simplicity of the WHT to achieve a high-throughput, low-power implementation suitable for real-time 6G high-mobility scenarios.

TABLE I
COMPUTATIONAL COMPLEXITY COMPARISON

Metric	OTFS (FFT-based)	OTSM (WHT-based)
Complex Multiplications	$NM \log_2 N$	**Zero**
Complex Additions	$NM \log_2 N$	$NM \log_2 N$
DSP Slice Usage	High	**Minimal**

TABLE II
RESOURCE UTILIZATION ($N = 128, M = 64$)

Resource	Available	Used (OTSM)	Utilization %
LUTs	303,600	82,936	27.32%
Registers	607,200	29,392	4.84%
BRAM (18Kb)	1030	80	7.77%
DSPs	2800	9	0.32%

C. Computational Complexity

Table I compares the arithmetic requirements of OTSM vs. OTFS for a frame of NM symbols.

D. Synthesis Results

The design was synthesized for the Xilinx Kintex-7 (XC7K325T) FPGA. At a clock frequency of 250 MHz, the OTSM transmitter achieves a throughput of 2 Gbps.

E. Flowchart and Explanation of WHT

The flowchart of the proposed WHT module represents a sequential finite state machine (FSM) that efficiently performs in-place transform computation using iterative butterfly operations. Initially, in the *IDLE* state, the system waits for the start signal, after which it transitions to the *INPUT* state where incoming samples *data_in* are stored in memory *mem* using the counter *in_cnt*. Once all N input samples, where **N** is a power of 2 are loaded, the computation begins with the initialization of key control variables. **stage** defines butterfly span, **a** defines intra-group index, and **b** defines inter-group index.

In the *FETCH* state, two operands x and y are read from memory locations determined by $b + a$ and $b + a + stage$, representing butterfly pairs. Then the main WHT butterfly operation is computing by taking sum $(x + y)$ and difference $(x - y)$ and writing them back to the same memory

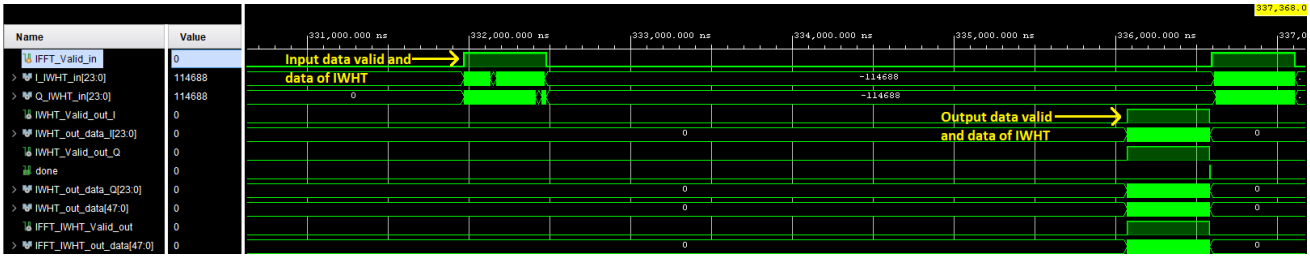

Fig. 5. FPGA based simulation featuring transmitter side Valid and data for input and output.

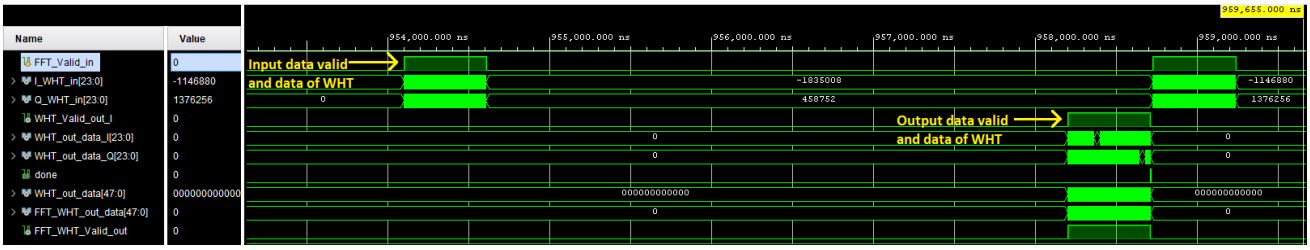

Fig. 6. FPGA based simulation featuring receiver side Valid and data for input and output.

locations, enabling in-place computation. The loop control using *a* and *b* ensures that all butterfly pairs within a stage are processed, while *stage* is doubled iteratively to span larger data segments, following the radix-2 WHT structure. Once all stages are completed, the FSM transitions to the *OUTPUT* state, where transformed data is sequentially read using *out_cnt*, with *data_out_valid* indicating valid output and *done* signaling completion. This structured control flow enables efficient hardware realization of WHT with minimal memory overhead and deterministic latency, making it suitable for FPGA-based OTSM transceiver implementations.

F. Result and Discussions

The proposed OTSM transceiver along with the WHT module was implemented using Verilog and functionally verified through simulation (Fig. 5 and Fig. 6). The input data sequence was processed through the transmitter chain, where WHT-based modulation and mapping were performed, followed by corresponding demodulation and inverse processing at the receiver. The simulation waveforms confirm correct state transitions and data flow. The figure shows the data valid and data of input and output of IWHT and WHT for transmitter and receiver side respectively.The obtained output matches the expected transmitted symbols, validating the correctness of the design. Additionally, the plotted results demonstrate proper reconstruction of the signal with minimal distortion, indicating robustness of the implemented architecture. These results verify that the proposed FPGA-based OTSM transceiver achieves reliable performance with efficient hardware utilization.

IV. Conclusion

This paper presented a robust FPGA-based implementation of an OTSM transceiver architecture. By leveraging the WHT for domain mapping, the proposed design successfully circumvents the high arithmetic complexity associated with traditional FFT-based doubly-selective waveform architectures. The implementation results demonstrate that arranging symbols in the delay sequency domain, coupled with hardware efficient butterfly processing, provides significant advantages in terms of reduced logic-gate utilization and deterministic processing latency. Furthermore, the architecture maintains high resilience to severe Doppler spreads and multipath fading, characteristic of high-mobility wireless environments. These findings validate OTSM as a technically viable and hardware-efficient candidate for real-time physical-layer realization in next-generation B5G and 6G communication systems.

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