Low-power Architecture for Wideband Spectrum Sensing

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***Abstract*—In this paper, a novel power efficient architecture for detecting the spectral holes over a very high bandwidth is proposed. Wideband spectrum sensing poses serious challenges for low-power spectrum sharing radios (for e.g., cognitive radio) which cannot afford to use high-rate Analog-to-Digital Converters (ADCs) to sample the signals at Nyquist rate and process them digitally thereby spending a lot of power. Here we propose an analog/mixed signal topology for wideband spectrum sensing that replaces the conventional Nyquist ADCs and digital Fast Fourier Transform (FFT) core with a bank of Sample and Hold (S/H) circuits, each operating at sub-Nyquist rate, and an all-analog FFT processor. The results show that even though sub-optimal analog processing leads to worse spectral reconstruction compared to conventional techniques, good detection performances can be achieved along with a substantial reduction in the power consumption.**

I. Introduction

The frequency spectrum is a scarce resource and has to be utilized efficiently to foster innovations in wireless communications. Spectrum sharing radios enable this by supporting secondary spectrum usage, coexistence, and dynamic spectrum access by sensing the spectral occupancy and adaptively using the free frequency band for a certain duration without affecting the performance of the primary radio link [1]. In case of low-power radios, spectrum sensing is usually an overhead for the radio and should consume minimal power. Normally spectrum sensing in radios is achieved by,

- *Narrowband sensing*: Over a given wide band of interest, spectrum sensing is performed over individual narrow bands either sequentially or at random [2] until a free channel is found. The disadvantage of this method is the latency in finding a free band (which is high when the spectrum is less sparse) and the inherent power consumption as the full receiver chain has to be powered each time a channel is sensed.
- *Wideband sensing*: The entire band of interest is processed at once to find a free channel, with either a single Nyquist rate Analog-to-Digital Converter (ADC) or a bank of sub-Nyquist rate ADCs, both followed by digital processing. These typically consume a lot of power, and low-power radios cannot afford it. Compressive Sampling or Compressed Sensing (CS), is a recently emerging approach for wideband sensing [3], which samples the signal at the information rate rather than at the Nyquist rate. CS generally requires knowledge of the sparsity level (ratio of the number of busy channels to the total number of channels). Usually, detection with CS is preceded by a coarse or a fine spectrum estimation. Estimating the spectrum using CS generally requires ℓ_1 optimization and is usually carried out using high-complexity recursive algorithms (e.g., the interior point linear program solver of [4]) or suboptimal algorithms such as Orthogonal Matching Pursuit (OMP) may be used to solve this convex problem. The performance of CS based methods is similar to that of Nyquist rate sampling when the spectrum is not so sparse.

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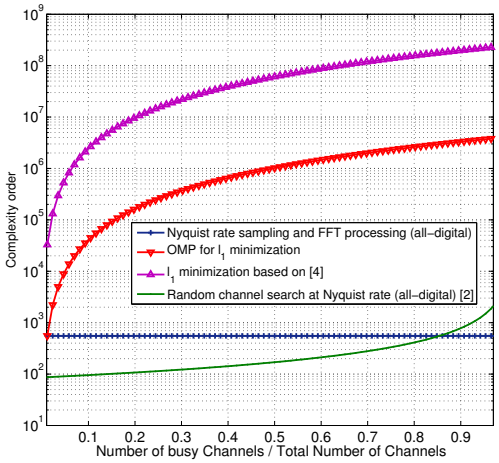

Fig. 1: Complexity order of existing algorithms.

The computational complexity order of existing sensing algorithms for different sparsity levels is shown in Fig. 1. Even though Nyquist rate sampling appears to be the best compromise for wideband sensing, it requires high-rate ADCs and outputs a large number of samples. Performing all-digital processing on such a large number of Nyquist rate samples consumes a lot of power. In [2], the complexity is reduced by computing only the required frequency domain coefficient instead of all the coefficients. Unfortunately this still needs a

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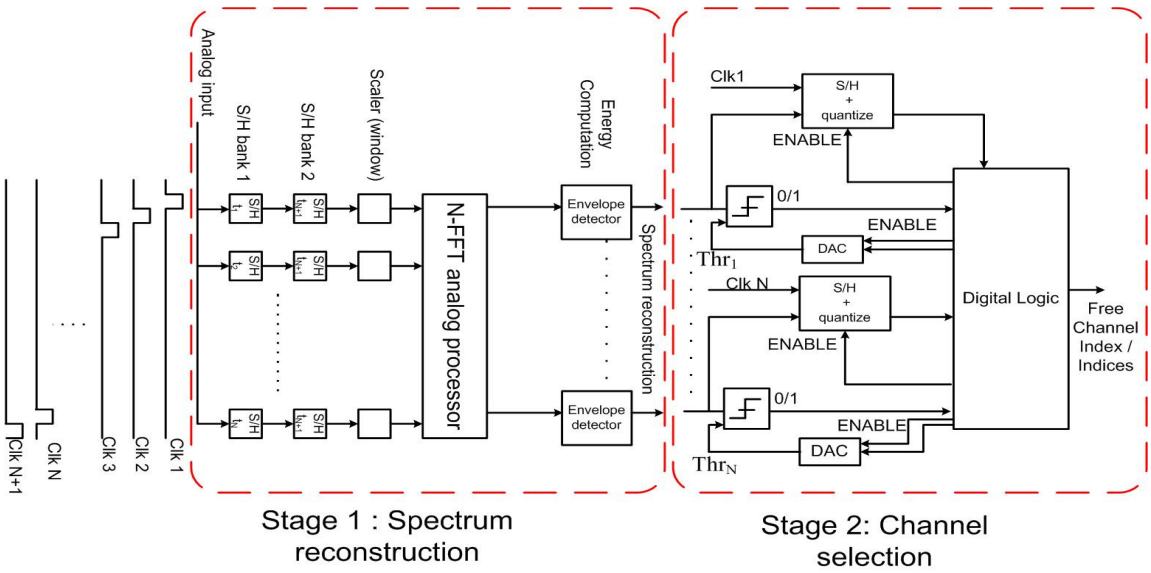

Fig. 2: Architecture for low-power wideband spectrum reconstruction and channel selection using an analog FFT.

high-rate ADC. Hence, there is a need for wideband sensing algorithms with lower complexity or lower power consumption.

A. Motivation

The idea of analog FFT processors was initially proposed for low-power Orthogonal Frequency Division Multiplexing (OFDM) receivers operating at Giga-samples per second [5]–[8], to reduce the total information processed by the ADCs, and make them power efficient. This motivates the proposed architecture, pushing the conventional ADC and digital processing to the analog domain, at the same time saving a considerable amount of power. In addition, a periodogram can be reconstructed in the analog domain using envelope detectors, which in turn provides averaging for each energy estimate and reduces the effect of fading.

Here, we use an analog/mixed signal topology that replaces the conventional Nyquist rate ADCs and digital Fast Fourier Transform (FFT) core with a bank of Sample and Hold (S/H) circuits, each operating at sub-Nyquist rate, and an all-analog FFT processor. The proposed low-power cross-layered system architecture is used for wideband coarse spectrum reconstruction and free channel selection.

Typically in wideband spectrum sensing, detecting both weak and strong signals (e.g., separated by 50 dB) requires a large dynamic range for the ADCs, to accommodate strong signals while still providing sufficient quantization performance for the weak signals. The power consumption of an ADC increases linearly with the sampling frequency and exponentially with the resolution [9]. This makes the front-end circuitry more complex or high-power (as in [10]) for sensing signals with a large dynamic range. Processing in the analog domain, using S/H circuits offers a low-complexity solution to mitigate the ADC resolution issues associated with the wideband occupancy detection.

B. Contributions

In this paper, we propose a low-power cross-layered system architecture, for wideband coarse spectrum reconstruction and free channel selection. The main contribution of the paper is to use the analog/mixed-signal based FFT processors for coarse spectral reconstruction and occupancy detection. This architecture leads not only to significant power saving by doing most of the processing in the analog domain and going to digital domain only for low-rate operations. The proposed architecture is based on a bank of Sample and Hold (S/H) circuits, analog FFT processing, low-power envelope detectors for spectrum reconstruction, and analog decision thresholds for channel selection. An estimate of the power consumption for both the proposed and the conventional all-digital processing method is provided.

The remainder of the paper is organized as follows. We present the proposed architecture is Section II. In Section III, we discuss the system model and formulate the hypothesis testing problem for occupancy detection. The performance of the proposed technique in terms of spectrum reconstruction and detection is discussed in Section IV, along with an estimate of the power consumption. The conclusions are provided in Section V.

Notation: We use bold upper and lower case letters for matrices and column vectors, respectively. (i, j)th element of a matrix $\mathbf{A}$ is denoted by $[\mathbf{A}]_{ij}$. $(\cdot)^T$ stands for transpose operation.

II. Proposed System Architecture

The block diagram of the proposed architecture is illustrated in Fig. 2. The architecture comprises two stages, *stage 1* for coarse spectrum reconstruction and *stage 2* for channel selection. The analog input baseband signal after the Low-Noise Amplifier (LNA) is discretized using a bank of S/H

circuits indicated by S/H bank 1 in the block diagram. The S/H bank 1, consists of N S/H circuits respectively operating at clock (clk) clk1, clk2, ..., clk$N$. Each S/H circuit should operate at a rate, $\frac{2\times B}{N}$ to monitor a spectrum of B Hz. The second bank of S/Hs indicated by S/H bank 2, also consists of N S/H circuits and re-samples the data from the S/H bank 1, at clk$(N+1)$. The two banks of S/Hs are used to achieve a serial to parallel conversion, which is required for the N-FFT analog processor. The output of the S/H bank 2 is scaled to realize a time domain windowing (e.g., Hamming) to reduce spectral leakage. The N-FFT analog processor is an analog implementation of an N-point FFT. More details regarding the implementation of an analog FFT processor can be found in [5]. The outputs of the N-FFT analog processor are an evolution of N discrete frequency bins in time. Each of these N branches, are fed to N envelope detectors to compute the energy in each frequency bin. An envelope detector can be modeled as a squaring function followed by a low-pass filter. The N branches viewed together would result in a coarse spectrum reconstruction based on a modified periodogram. It should be noted that the low-power envelope detector after the analog FFT output helps reducing the multi-path and fading effects associated with spectrum sensing.

To find an empty channel in the spectrum, the output of the branches of the envelope detectors are compared to a threshold. The thresholds are set to achieve a maximum probability of detection P_d (to detect a channel as busy, when the channel is indeed busy) subject to a probability of false alarm P_{fa} (decision that a channel is occupied, when the channel is in fact free) constraint. The noise power estimation and threshold updates are controlled via digital logic and could be performed during the initialization stage. When the threshold has to be updated, the output of the envelope detector is quantized whenever a channel is detected as free. This quantized output is used in the digital logic to compute a new threshold. The threshold can be different or can be the same for all the frequency bins. The blocks used to set the threshold are i) S/H + quantize and ii) Digital-to-Analog Converter (DAC), can be reused in a time interleaved manner for all the N branches to conserve power. The output of the digital logic at *stage 2* will be the indices of the free channels. It should be noted that, only in *stage 2* for computing the threshold, we go to the digital domain, since both the number of samples to be processed and the frequency of processing (e.g., during the initialization) are small.

III. Detection

A. System model

The signal at the k^{th} branch (indicating the k^{th} frequency bin) before the envelope detector during time m is denoted by y_{km}. These are collected for M time instances in the $M \times 1$ vector $\mathbf{y}_k$ given by $\mathbf{y}_k = [y_{k1}, \quad y_{k2}, \ldots, \quad y_{kM}]^{\mathrm{T}}$. At time m and frequency k, the signal is denoted by $x_{km} \sim \mathcal{N}(0, \sigma_x^2)$ and the noise by $v_{km} \sim \mathcal{N}(0, \sigma_v^2)$. The device mismatch for the N-FFT analog processor is modeled as Gaussian noise as illustrated in Fig. 3 with a variance δ_N^2 and is denoted at time

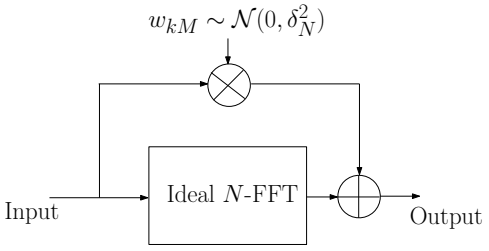

Fig. 3: Mismatch model for CMOS based analog FFT [5].

m and frequency k by the Random Variable (RV) w_{km}. The mismatch model accounts for the noise propagation from stage to stage in the analog circuitry which is very sensitive to the radix size (full-radix FFT being less sensitive to the device mismatch) [5]. The mismatch model at the k^{th} branch during time m will result in $w_{km}v_{mk}$ for the noise and in $w_{km}x_{mk}$ for the signal. These are collected for M time instances in the $M \times 1$ vectors $\mathbf{q}$ and $\mathbf{r}$ respectively given by

$$\mathbf{q} = \left[w_{k1}v_{1k}, w_{k2}v_{2k}, \ldots, w_{kM}v_{nk}\right]^{\mathrm{T}},$$

$$\mathbf{r} = \left[w_{k1}x_{1k}, w_{k2}x_{2k}, \ldots, w_{kM}x_{nk}\right]^{\mathrm{T}}.$$

Let $\mathbf{f}_k$ be the $1 \times N$ vector indicating the k^{th} row of a Discrete Fourier Transform (DFT) matrix, $[\mathbf{F}]_{kn} = \exp(-\frac{2\pi\iota(k-1)(n-1)}{N})$, with $k, n = 0, \ldots, N-1$ and $\iota = \sqrt{-1}$. Let $[\mathbf{X}]_{mk} = x_{mk}$ and $[\mathbf{V}]_{mk} = v_{mk}$, with $m = 1, \ldots, M$ and $k = 1, \ldots, N$, be the $M \times N$ signal and noise matrices, respectively, representing M (number of time snapshots) vectors of N values discretized by the S/H bank.

The spectrum sensing engine decides on the occupancy of the channel by solving the binary hypothesis testing problem between the hypothesis $\mathcal{H}_0$ indicating the channel is free and hypothesis $\mathcal{H}_1$ which indicates that the channel is occupied. The hypothesis testing problem is given by

$$\begin{aligned} \mathcal{H}_0 &: \mathbf{y}_k = \mathbf{V}\mathbf{f}_k^T + \mathbf{q}, \\ \mathcal{H}_1 &: \mathbf{y}_k = \mathbf{X}\mathbf{f}_k^T + \mathbf{V}\mathbf{f}_k^T + \mathbf{r} + \mathbf{q}. \end{aligned} \tag{1}$$

This system model can also be viewed as a detection problem with multiplicative Gaussian noise.

B. Probability of false alarm and detection threshold

In this paper, the Neyman-Pearson criterion is considered, where we set a constraint on the probability of false alarm P_{fa} and determine the detection threshold γ_{th}. The corresponding probability of detection P_d for different Signal to Noise Ratios (SNRs) is shown through simulations. To determine the threshold for a certain P_{fa}, we next derive the distribution of the signal at the k^{th} branch after the envelope detector (indicating its energy, $E = \sum_{m=1}^{M}(y_{km})^2$) under the $\mathcal{H}_0$ hypothesis.

The entries of $\mathbf{q}$ have a normal product distribution, i.e., $q_i \sim \mathcal{N}(0, \delta_N^2) \cdot \mathcal{N}(0, \sigma_v^2)$, with $i = 1, \ldots, M$. To simplify the derivation, we approximate the normal product distribution with a sum of two Gaussian functions denoted by the Probability Density Function (PDF) f_U. The normal product

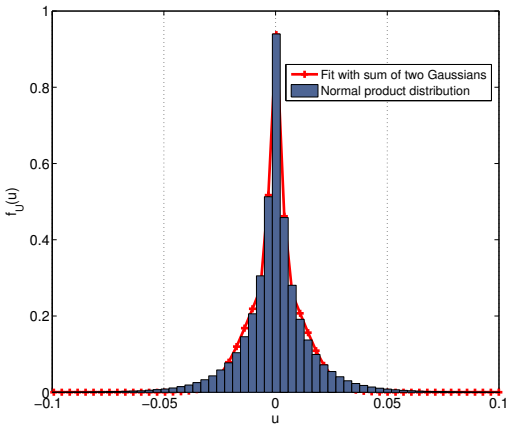

Fig. 4: Normal product distribution vs. the best fit with a sum of two Gaussian functions.

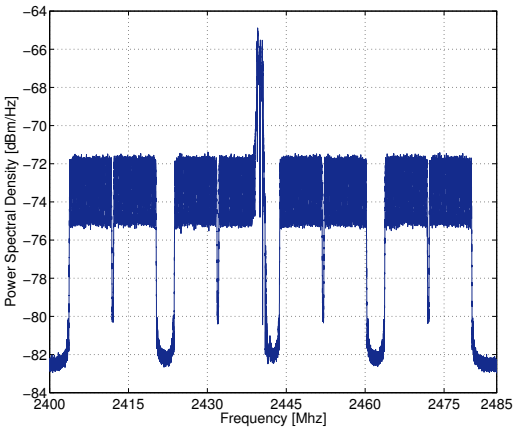

Fig. 5: Spectrum with four IEEE 802.11g/WiFi nodes and 1 IEEE 802.15.4/Zigbee node.

distribution after the approximation by a sum of two Gaussian functions is given by the PDF

$$f_U(u) = \frac{1}{\sqrt{\pi}(a_1\sigma_1 + a_2\sigma_2)}(a_1 \exp -(\frac{u}{\sigma_1})^2 + a_2 \exp -(\frac{u}{\sigma_2})^2), \tag{2}$$

and the PDF of the noise is given by

$$f_V(v) = \frac{1}{\sqrt{\pi}(\sigma_3)} \exp -(\frac{v}{\sigma_3})^2, \tag{3}$$

where a_1 and a_2 are the weights, and σ_1 and σ_2 are the standard deviations of the Gaussian functions in (2); and $\sigma_3 = \sqrt{2}\sigma_v$ is just a scaled standard deviation of the noise.

The simulations in Fig. 4 show that the sum of two Gaussian functions is a good approximation for a normal product distribution. The RVs $u_1, u_2, \ldots, u_M$ are independently and identically distributed (i.i.d.) with PDF f_U. Hence, the RV $q_i \approx u_i$, with $i = 1, \ldots, M$. The RVs $v_1, v_2, \ldots, v_M$ are i.i.d. with the PDF f_V. E can be modeled as a process defined by the RV, $z = \sum_{i=1}^{M}(q_i + v_i)^2 \approx \sum_{i=1}^{M}(u_i + v_i)^2$.

Next, we derive the PDF $f_Z(z)$. To do this, we first derive the PDF $f_Z(z)$ for $M = 1$. Using the convolution and square law property, we can write

$$f_Z(z|M=1) = \frac{1}{\sqrt{\pi z(a_1\sigma_1 + a_2\sigma_2)}} (\frac{a_1\sigma_1}{\sqrt{\sigma_1^2 + \sigma_3^2}} \exp(\frac{-z}{\sigma_1^2 + \sigma_3^2}) + \frac{a_2\sigma_2}{\sqrt{\sigma_2^2 + \sigma_3^2}} \exp(\frac{-z}{\sigma_2^2 + \sigma_3^2})). \tag{4}$$

The characteristic function of the RV z for $M = 1$ will be

$$\bar{\Omega}_Z(\omega) = \int_{-\infty}^{\infty} \exp(iz\omega) f_Z(z|M=1)dz = \frac{1}{\sqrt{a_1\sigma_1 + a_2\sigma_2}} (\frac{a_1\sigma_1}{\sqrt{1 - i(\sigma_1^2 + \sigma_3^2)\omega}} + \frac{a_2\sigma_2}{\sqrt{1 - i(\sigma_2^2 + \sigma_3^2)\omega}}). \tag{5}$$

Hence, the characteristic function of the RV z for any M will be $\Omega_Z(\omega) = (\bar{\Omega}_Z(\omega))^M$.

The PDF $f_Z(z)$ can be then written as

$$f_Z(z) = \frac{1}{2\pi} \int_{-\infty}^{\infty} \exp(-iz\omega)\Omega_Z(\omega)d\omega. \tag{6}$$

Using binomial theorem, [11], and after some mathematical manipulations, the PDF $f_Z(z)$ is given by

$$f_Z(z) = \frac{\exp(\frac{-z}{\alpha})z^{(\frac{M}{2}-1)}}{\Gamma(\frac{M}{2})(\varphi_1 + \varphi_2)^M} \sum_{k=0}^{M} \binom{M}{k} (\frac{\varphi_1}{\sqrt{\alpha}})^{M-k} \left(\frac{\varphi_2}{\sqrt{\beta}}\right)^k {}_1F_1\left(\frac{k}{2}; \frac{M}{2}; \frac{(\beta-\alpha)z}{\alpha\beta}\right). \tag{7}$$

where, $\Gamma(\theta) = \int_0^\infty \tau^{\theta-1}\exp(-\tau)d\tau$ is the Gamma function, and ${}_1F_1(a;b;z) = \frac{\Gamma(b)}{\Gamma(b-a)\Gamma(a)} \int_0^1 \exp^{zt} t^{(a-1)}(1-t)^{(b-a-1)}dt$ is the confluent hypergeometric function of the first kind.

Then, the probability of false alarm can be written as

$$P_{fa} = Pr(E \geq \gamma_{th}|\mathcal{H}_0) = \int_{\gamma_{th}}^{\infty} f_Z(z)dz. \tag{8}$$

The integral (8) can be solved numerically and the threshold for a certain P_{fa} can be obtained by solving the lower tail probability using Newton's method and can be computed off-line.

IV. Performance Evaluation and Analysis

A. Simulations

A network in the 2400 MHz ISM band with 86 frequency bins of 1 MHz resolution centered at f_c = 2400, 2401, . . . , 2485 MHz is simulated. The simulated scenario has four WiFi (IEEE 802.11g) nodes centered at 2412, 2432, 2452, 2472 MHz respectively and one Zigbee (IEEE 802.15.4) node centered at 2440 MHz. An illustration is provided in Fig. 5, which is constructed with a high resolution FFT (FFT length = 183430). The signals considered are present at all times with a fixed transmit power.

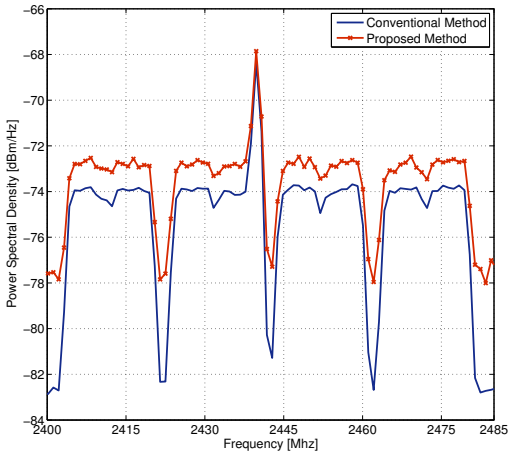

Fig. 6: Spectrum reconstruction using both the conventional and proposed method with a 128-point FFT.

The proposed system architecture is simulated such that the resolution of the samples mimic the analog signal, and the all-analog FFT is realized using the mismatch model as in Fig. 3 with $\delta_N^2 = 52.3$ for the 128-point FFT processor. The spectrum reconstruction with the conventional (all-digital) method using a Nyquist rate ADC and a 128-point digital FFT, as well as the spectrum reconstruction obtained at *stage 1* of the proposed architecture are shown in Fig. 6. It can be seen that using the proposed architecture a coarse spectrum estimate can be obtained, where the losses in dynamic range compared to the conventional method can be traded for a considerable power saving. It should also be noted that the ultimate goal is to detect occupancy of the spectrum.

Fig. 7 shows the spectrum reconstruction performance in terms of the Mean Squared Error (MSE) between the high resolution FFT and the digital 128-point FFT for the conventional method and between the high resolution FFT and the 128-point analog FFT for the proposed method. The analog processing results in a deterioration of the signal strength, and introduces some noise between the stages.

An actual channel occupancy of around 80% with a frequency resolution of 1 MHz shown in Fig. 8, is used to evaluate the detection performance. The detection performance in terms of P_{fa} and P_d for different SNRs is shown in Fig. 9. The threshold is set so as to maintain a P_{fa} below 5%, so that the P_d of the two methods can be compared. With the proposed architecture, a detection performance comparable to that of the conventional method can be achieved, with losses below 1 dB in the observed SNR range.

B. Power consumption comparison: conventional vs. proposed

In this section, we compare the power consumption of the conventional all-digital approach, which involves sampling at Nyquist rate using a high-rate 8-bit ADC, with the application of an FFT using an 8-bit 128-point digital FFT processor. An 8-bit ADC based on 90nm CMOS technology

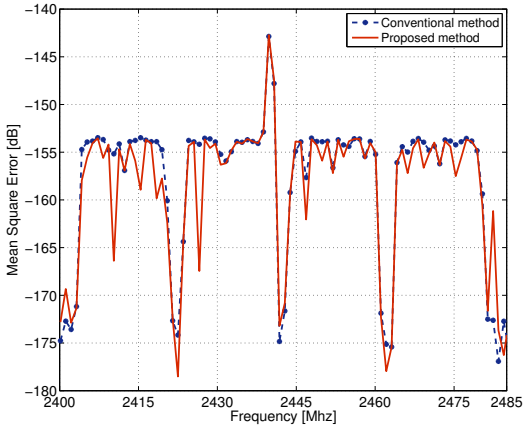

Fig. 7: Mean squared error of the spectrum reconstruction.

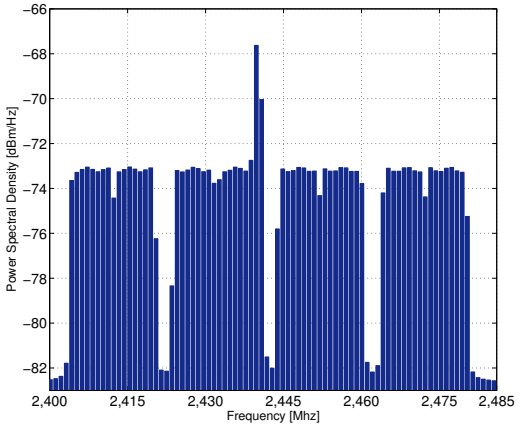

Fig. 8: Smoothed periodogram indicating 86 frequency bins, with 1 MHz frequency resolution.

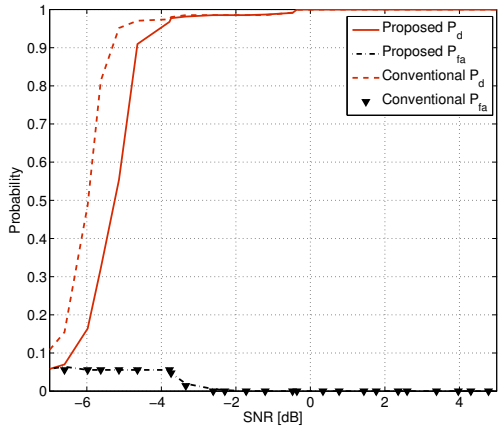

Fig. 9: Detection performance.

is considered. The power consumption of the ADC is approximately $27\mu W/10$ Megasamples/second, i.e., 2.7pJ/conversion

step [12]. The 8-bit state-of-the-art energy aware digital FFT processor proposed for low-power sensor nodes [13] consumes around 33nJ/FFT (a scaling factor of 0.66^3 [14] for scaling the energy from 180nm to 90nm CMOS technology is used).

The proposed method uses S/H circuits which can be estimated to consume 10% of the ADC's power on average [15]. The analog 128-point FFT processor requires 512 differential inputs and 7 stages for a radix-2 implementation of the butterfly structure, and the number of multipliers from the 128-FFT stage to the 8-FFT stage would be about 576 [5]. With a bias current of 100nA and $V_{dd} = 1.2V$ (for 90nm CMOS technology), the power consumption would be of the order of $(512\times7+576)(0.12\mu W) = 0.5mW$, and considering an FFT processor speed of 1 MHz, the energy/FFT will be 500 pJ/FFT. A summary of the comparison of the estimated power between the proposed and conventional method is given in Table I. In this example, it can be clearly seen that with the proposed architecture, the power consumption could be reduced by a factor of 50, compared to the conventional all-digital approach.

TABLE I: Estimated energy and power consumption for 128-point FFT systems.

Estimated	**Conventional**	**Proposed**
pJ/conversion	(ADC) **2.7**	(S/H) **2× 0.27 = 0.54**
pJ/FFT	(Digital) **33000**	(Analog) **≈500**
Power (mW)	(ADC + Digital FFT) **33.7**	(S/H + Analog FFT) **≈0.64**

In the proposed architecture, to realize the periodogram estimate and channel selection, additional power is consumed. Envelope detectors can consume a power below 1.5μW for state-of-the-art designs [16]. On the other hand, for the conventional method, these steps are done digitally using different algorithms with different complexity orders, as discussed in Section I.

In the proposed architecture we choose energy detector, since it is simple and of low-complexity. As any energy detector, this system also suffers from noise uncertainty and SNR wall issues. To enhance the performance in the low-SNR regimes, a two-stage sensing can be performed as suggested in the literature [17]. Typically, the second stage performs feature detection (e.g., cyclostationarity, pilot-tone detection) on the detected free narrowband channels, to improve the performance at low SNRs.

V. Conclusions

In this paper, we have proposed an architecture for low-power wideband spectrum sensing. With the proposed architecture a large portion of the spectrum (e.g., 128 MHz) can be sensed at once to obtain a coarse estimate of the spectrum and/or search for an empty channel. The major high-power consuming processes are pushed to the analog domain which include the high-rate ADC and the digital FFT operations, which are replaced by a bank of S/H circuits and an analog FFT processor, respectively. We do this to avoid digital processing of a large number of Nyquist rate samples and instead perform the majority of the processing in the analog domain. We only go to the digital domain for the computation of the threshold, when both the number of samples to be processed and the processing intervals are relatively small. The simulation results show that even though analog processing leads to worse spectrum reconstruction compared to the conventional method, a good detection performance can still be achieved with a substantial reduction in power consumption.

VI. Acknowledgement

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